2. *MAIN FRAME. CIRCUIT DESCRIPTION*

2.1 GENERAL

This chapter describes the PM 3632 main system.
For an overall understanding of the functioning of all the separate blocks, refer to the block diagram (figure 1.2) first.
A more detailed block diagram is shown in figures 2.1 and 2.2 (microcomputer and analyzer function respectively).
This block diagram will not be explained in detail, but can be used together with the circuit descriptions.

These circuit descriptions contain no unit drawings. All component numbers are printed on the pc board which makes them self-explanatory. How all the pc boards are connected is shown in figure 2.3.
Figure 2.4 shows all the connectors at the capture board and the front panel with all the signal lines that are connected via these connectors.

In all circuit descriptions, a * behind a signal name indicates that it is low active. In the diagrams, the corresponding signalname has a horizontal bar above it.

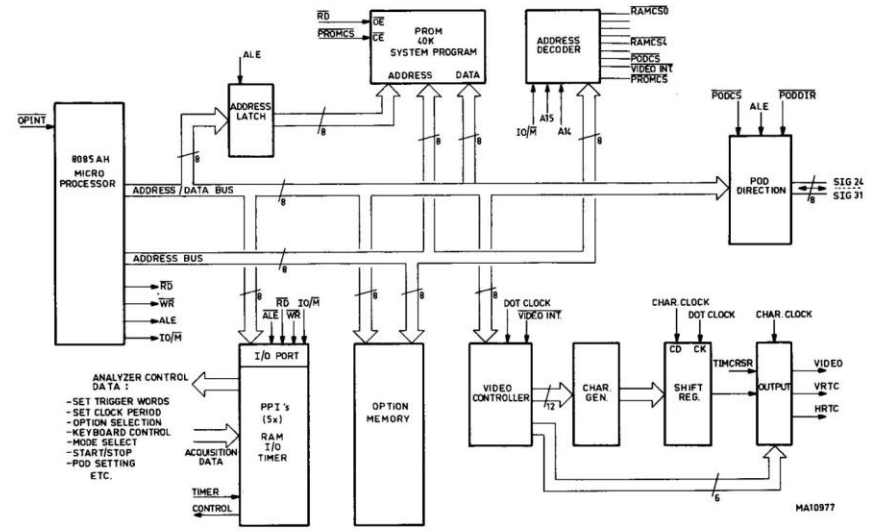

Figure 2.1 : Micro computer, block diagram.

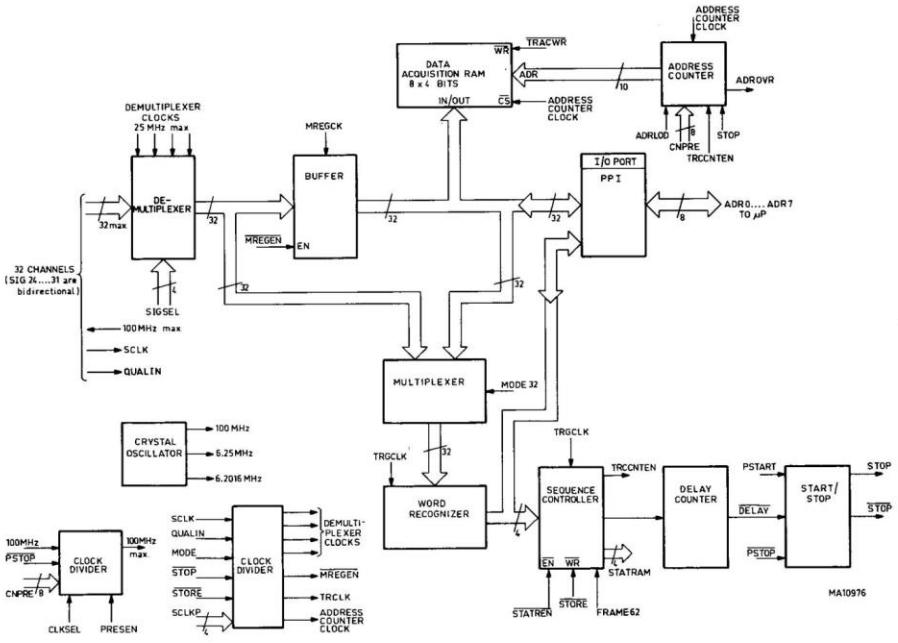

Figure 2.2 : Analyzer functions, block diagram.

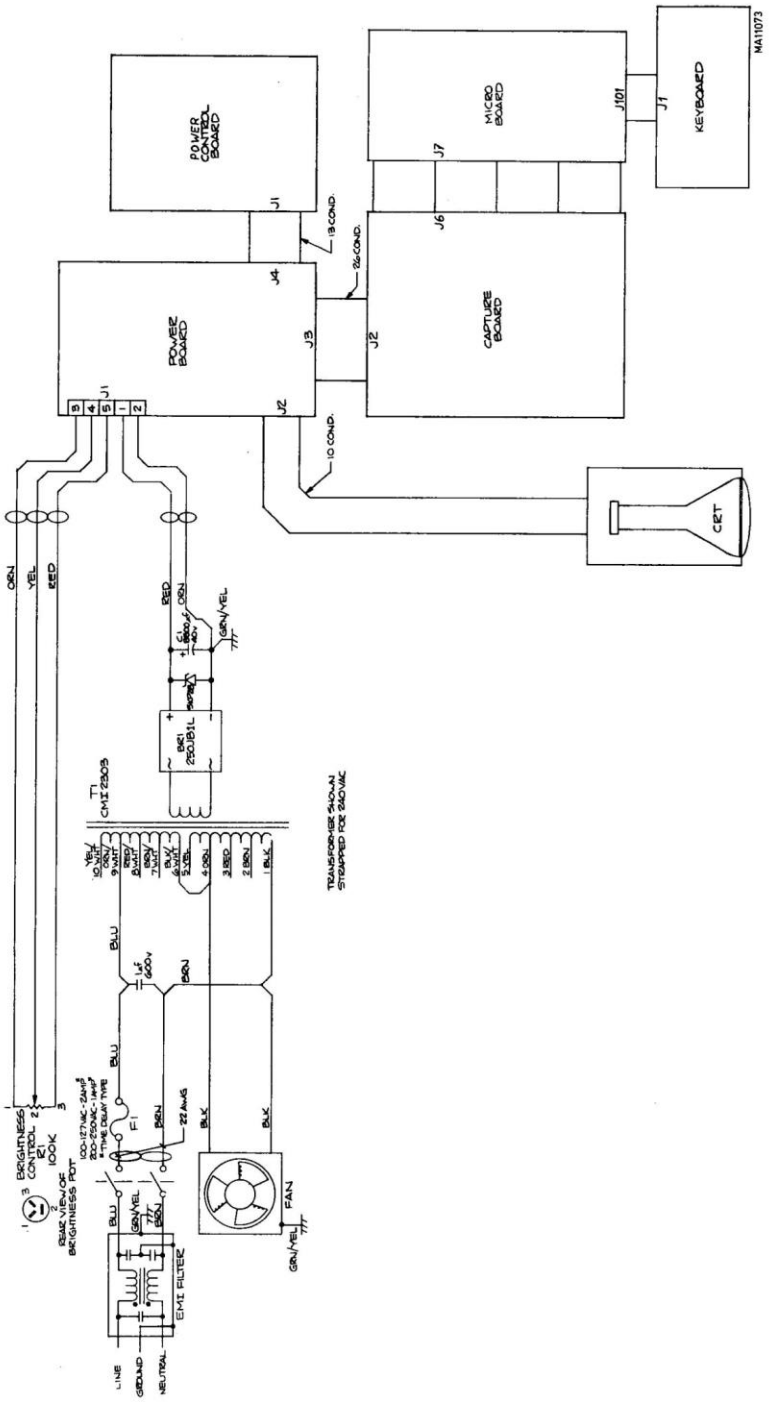

Figure 2.3 : Interconnection between units.

LIST OF SIGNAL NAMES (diagram 1)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
6.2016 MHz	Video and uP clock	3	1	
A10	Addressline 10	2	1	
A11	Addressline 11	2	1	
A12	Addressline 12	2	1	
A13	Addressline 13	2	1	
A14	Addressline 14	2	1	
A15	Addressline 15	2	1	
AD0	Address/data line 0	2	1	
AD1	Address/data line 1	2	1	
AD2	Address/data line 2	2	1	
AD3	Address/data line 3	2	1	
AD4	Address/data line 4	2	1	
AD5	Address/data line 5	2	1	
AD6	Address/data line 6	2	1	
AD7	Address/data line 7	2	1	
ADRLOD	Address counter load	2	1	
ALE	Address latch enable	2	1	
BFCLKOUT	Buffered int. sampling clock, out	3	1	
BFPODSEL0	Buffered pod select 0	3	1	
BFPODSEL1	Buffered pod select 1	3	1	
BFPODSEL2	Buffered pod select 2	3	1	
BFPODWRT*	Buffered pod write	3	1	
CNPRE0	Counter preset 0	2	1	
CNPRE1	Counter preset 1	2	1	
CNPRE2	Counter preset 2	2	1	
CNPRE3	Counter preset 3	2	1	
CNPRE4	Counter preset 4	2	1	
CNPRE5	Counter preset 5	2	1	
CNPRE6	Counter preset 6	2	1	
CNPRE7	Counter preset 7	2	1	
DELAY*	Final delay finished	3	1	
DLYCLK	Final delay counter clock	6	1	
EN62*	Enable 62 channel mode	2	1	
FRAME62	62 channel mode, frame indication	5	1	
HRTC	Horizontal retrace	2	1	
IO/M*	Input,output/ memory	2	1	
MODE 4*	4channel mode	2	1	
MODE32*	32 channel mode	2	1	
OP0SEL*	Select option slot 0	3	1	
OP1SEL*	Select option slot 1	3	1	
OP2SEL*	Select option slot 2	3	1	
OPINT*	Option interrupt	21,22,23	1	?
P00CS*	Chip select pod buffer	2	1	
PSTOP*	Pushbutton STOP depressed	2	1	
QUALIN	Qualifier in signal	10,13,16,18 19,20	1	?
RAMCS3*	RAM chip select 3	2	1	
RAMCS4*	RAM chip select 4	2	1	
RD*	Read signal	2	1	
READY	Ready	21,22,23	1	?
RESET OUT	Reset out signal	2	1	
S0	Status line 0	2	1	
S1	Status line 1	2	1	

LIST OF SIGNAL NAMES (diagram 1, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
SCLK	Selected clock	11,13,16,18 19,20	1	?
SCPEN*	Selected clock pulse enable	2	1	
SCPSEL	Selected clock pulse select	2	1	
SIO8IT	Serial input data, addresscounter	3	1	
SIG 0	Input channel 0	10,12,16,18 19,20	1	?
SIG 1	Input channel 1	10,12,16,18 19,20	1	?
SIG 2	Input channel 2	10,12,16,18 19,20	1	?
SIG 3	Input channel 3	10,12,16,18 19,20	1	?
SIG 4	Input channel 4	10,16,18,19 20	1	?
SIG 5	Input channel 5	10,16,18,19 20	1	?
SIG 6	Input channel 6	10,16,18,19 20	1	?
SIG 7	Input channel 7	10,16,18,19 20	1	?
SIG 8	Input channel 8	10,16,18,19 20	1	?
SIG 9	Input channel 9	10,16,18,19 20	1	?
SIG10	Input channel 10	10,16,18,19 20	1	?
SIG11	Input channel 11	10,16,18,19 20	1	?
SIG12	Input channel 12	10,16,18,19 20	1	?
SIG13	Input channel 13	10,16,18,19 20	1	?
SIG14	Input channel 14	10,16,18,19 20	1	?
SIG15	Input channel 15	10,16,18,19 20	1	?
SIG16	Input channel 16	11,16,18,19 20	1	?
SIG17	Input channel 17	11,16,18,19 20	1	?
SIG18	Input channel 18	11,16,18,19 20	1	?
SIG19	Input channel 19	11,16,18,19 20	1	?
SIG20	Input channel 20	11,16,18,19 20	1	?
SIG21	Input channel 21	11,16,18,19 20	1	?
SIG22	Input channel 22	11,16,18,19 20	1	?
SIG23	Input channel 23	11,16,18,19 20	1	?
SIG24	Input channel 24	3,11,13,16, 18,19,20	1	? BD
SIG25	Input channel 25	3,11,13,16, 18,19,20	1	? BD
SIG26	Input channel 26	3,11,13,16, 18,19,20	1	? BD
SIG27	Input channel 27	3,11,13,16 18,19,20	1	? BD
SIG28	Input channel 28	3,11,13,16, 18,19,20	1	? BD
SIG29	Input channel 29	3,11,13,16 18,19,20	1	? BD
SIG30	Input channel 30	3,11,13,16 18,19,20	1	? BD
SIG31	Input channel 31	3,11,13,16 18,19,20	1	? BD
SIGSEL0	Demultiplexers signal select 0	2	1	

LIST OF SIGNAL NAMES (diagram 1, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SIGSEL1	Demultiplexers signal select 1	2	1
SIGSEL2	Demultiplexers signal select 2	2	1
SIGSEL3	Demultiplexers signal select 3	2	1
SMODE	Select mode	2	1
STOP	Stop	6	1
STORE*	Store information	2	1
TAD8CLR*	Address counter, bit 8 clear	2	1
TAD8SET*	Address counter, bit 8 set	2	1
TAD9CLR*	Address counter, bit 9 clear	2	1
TAD9SET*	Address counter, bit 9 set	2	1
TRACWR*	Data aquisition memory write	2	1
TRCCNTEN	Address counter enable	6	1
TRCSTAT	Data qualification trigger switch	6	1
TRGCLK	Trigger clock	5	1
TRGREN*	Trigger enable	2	1
TWA0	Triggerword A, RAM 0	2,5	1 ?
TWA1	Triggerword A, RAM 1	2,5	1 ?
TWA2	Triggerword A, RAM 2	2,5	1 ?
TWA3	Triggerword A, RAM 3	2,5	1 ?
TWB0	Triggerword B, RAM 0	2,5	1 ?
TWB1	Triggerword B, RAM 1	2,5	1 ?
TWB2	Triggerword B, RAM 2	2,5	1 ?
TWB3	Triggerword B, RAM 3	2,5	1 ?
TWC0	Triggerword C, RAM 0	2,5	1 ?
TWC1	Triggerword C, RAM 1	2,5	1 ?
TWC2	Triggerword C, RAM 2	2,5	1 ?
TWC3	Triggerword C, RAM 3	2,5	1 ?
TWD0	Triggerword D, RAM 0	2,5	1 ?
TWD1	Triggerword D, RAM 1	2,5	1 ?
TWD2	Triggerword D, RAM 2	2,5	1 ?
TWD3	Triggerword D, RAM 3	2,5	1 ?
VBB		12	
VIDEO	Video signal	2	1
VRTC	Vertical retrace	2	1
WR*	Write signal	2	1

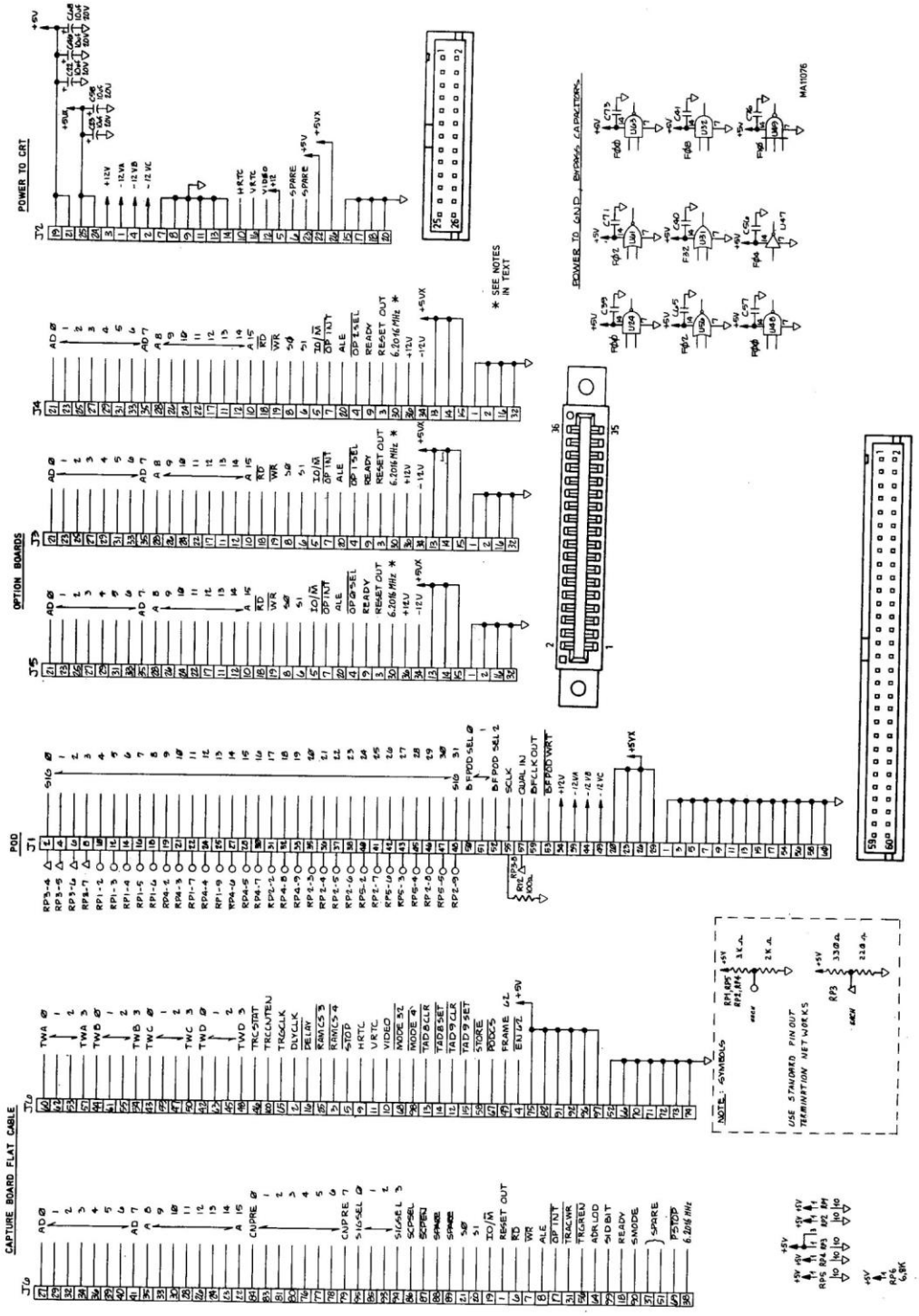

Figure 2.4 : Mainframe connectors (without power supply connectors) (1).

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2.2 CAPTURE BOARD

2.2.1 MICRO COMPUTER (AND USER INTERFACE) + CLOCK GENERATION.

Micro computer and user interface

The basic user interface, including keyboard and CRT handling, is provided by an 8085 NMOS microprocessor.
It and its associated circuits are located on the smaller part of the Capture Board and are illustrated in figure 2.6 and 2.7.
This portion of the machine can be subdivided into several sections:

- *ROM, RAM, and associated decoders which support the program execution.
- *An 8276 (small System CRT Controller) and associated components support the CRT.
- *Several 8155s (PPI's) are used to provide RAM, I/O and timers.

U120 is the 8085-AH main microprocessor (figure 2.6).
Its clock is supplied by a 6.2016 MHz signal produces elsewhere on the board (see clock generation). U101 inverts this clock to drive X2.
C135, R107 and associated diode provide a powerup reset to Pin 36 of the processor.

NOTE: In earlier instruments, the power-up capacitor is slightly too small. This causes sometimes a bad power-up for the uP, due to which the unit stays beeping after switch-on. A small increase (from 10 uF to 22 uF) of this capacitor (C135) will solve this problem. This will cause the unit to beep a little longer after power-up, but the power-up of the microprocessor is ok.
A nicer solution for solving the problem, is changing the power supply. For this, see chapter 2.4.

U101 buffers the interrupt line from the option cards and drives the INTR pin of the microprocessor.
The option card interrupt outputs are "wire-ored" to procedure the input of U101 (refer also to chapter 4).
Pin 7 of the microprocessor (RST 7.5) is driven by the stop logic (U114, see figure 2.14).
Pin 8 (RST 6.5) is driven by the CRT controller and interrupts for each new line of characters (signal BRDY : Buffer Ready).

The address & data bus outputs from the microprocessor are latched to form the lower address bus by U112 (by means of the ALE pulse).
These lower eight address bits and the next five higher address bits are applied directly to PROM sockets U113 and U121.
Chip selects for these devices are decoded uniquely and directly from the upper addresses by U115 and U117.
The address spaces for these PROMs are indicated on the circuit diagram (refer also to the memory map, figure 2.5).
U103 and the associated gates provide chip selects for the 8155s (PPI's) and the CRT controller (8276).

CRT controller.

The Chip select (CS*) input and the Command/Parameter (C/P*) input of the 8276 are only used to select the CRT controller during initialisation of the video screen. The microprocessor writes the information that defines the video screen into the command and parameter registers directly after power-up.
Inputs Buffer Select (BS*), WR* and RD* are used to fill the video buffer of the 8276 with a new line of characters..

U110, U111, and U133 provide a serial bit stream for the CRT monitor.
Each bit appearing on Pin 13 of U110 is a single dot on the CRT.
U133 outputs ASCII characters along with a row address (LL0-LL3).
1 Addressline (A9) of the character generator is used to divide it into two character sets; one for timing displays (some ASCII characters are replaced by timing characters) and one for other displays (ASCII characters).
These signals are used to address the character generator U111, whose outputs are the bits of one raster row of a character.
These bits are then shifted out by U110 to form the video display (the dot clock is 6.2016 MHz.in units connected to a 50 Hz mains).
A new character row is loaded into the shift register (U110) when signal VIDLOD (VIDEO LOAD, comes from U105) goes low.

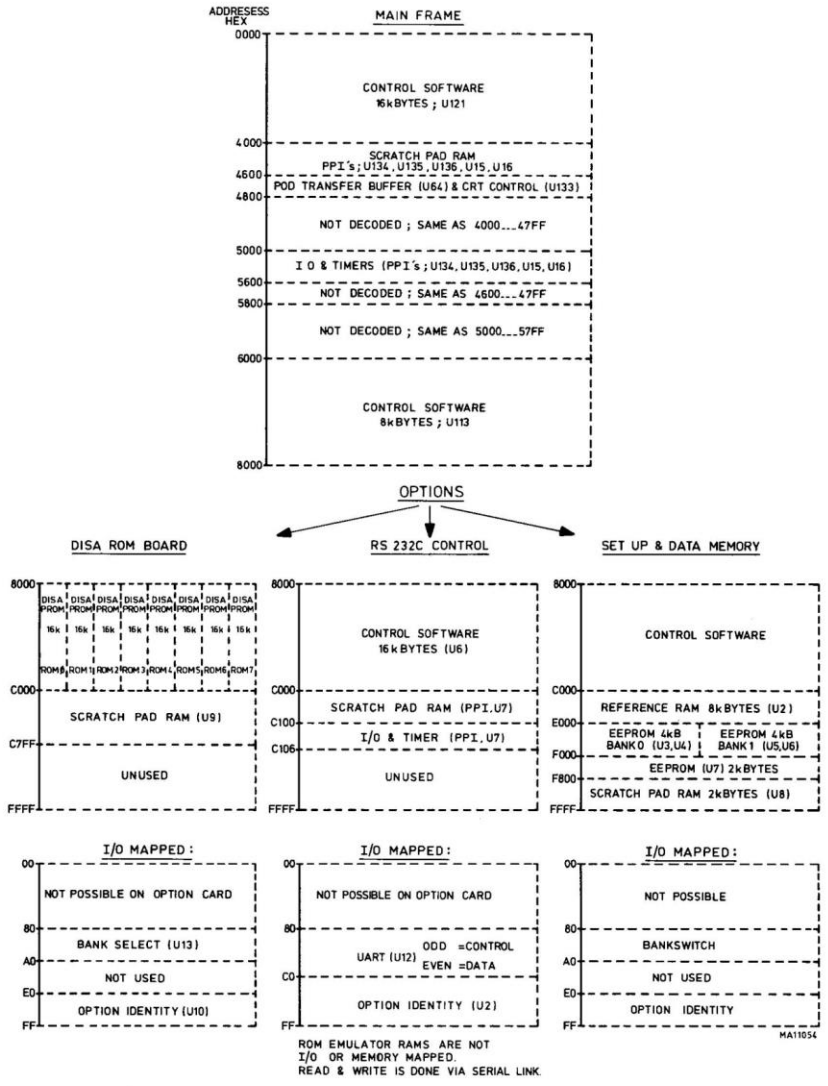


Figure 2.5 : Memory Map.

U119 synchonizes the CRT sync. signals and video attributes from the 8276 with the output of U110.
- VSP (video Suppression) : is used for switching on or off the video signal (blinking cursor).
- RVV (Reverse Video) : inverts the video signal.
- VRTC (Vertical retrace) : vertical synchronisation signal.
- HRTC (Horizontal retrace): horizontal synchronisation signal.
- GPA0, GPA1 (General Purpose Attributes): are used to define the vertical lengths of the cursor (timing display)

U127, Q101, and their associated components form four levels of video, including black.
The three signals-video, vertical sync. (VRTC), and horizontal sync. (HRTC)-- are connected to the CRT monitor.
The 8276 interrupts the microprocessor (BRDY) whenever its internal line buffer is empty.
The microprocessor then fills the buffer with a line of display characters.

U105 is used to derive the character clock (CCCK=VIDLOD) from the 6.2016 MHz dot clock (dot clock is 6.25 MHz for units connected to a 60 MHz. mains).
U105 also drives the cursor generators (Timers in 8155's), for which there are two similar circuits:
  one for the main cursor
  one for the reference cursors (time measurements)

Only the main cursor will be described here.
U125 is clocked to a "one" at the beginning of each line (by means of HRTC), which enables clocks to the timer in U134 via U115. Signal TRACGAT0 and the clock signal coming from U1050B generate four clock pulses in one character.
When the timer expires, U125 will clock to a "zero", again stopping timer clocks.
U114 delays this signal slightly, and U108 decodes the time between these two events as the cursor time (2 dots).
The two cursor signals are mixed at U107 Pin 3.
(The other circuit is similar, but uses two timers so the cursor width can be varied for time measurement displays.)

There are five 8155s on the microprocessor bus; each contains 256 bytes of RAM, a timer circuit, and 22 bits of I/O (see figure 2.7 also).
8155s demultiplex their own address from the processor data bus, and must be provided with the ALE signal.
Signal IO/M* (A12) indicates whether the RAM or the I/O parts are addressed.
Most I/O signals and timers will be described later along with the circuits they are used in.

Pins 29-31 of PPI U136 drive U132, which decodes them for row selects for scanning the keyboard.
The columns on the keyboard matrix are then returned to Pins 1, 2, 5, 37, 38 and 39 of U136 to complete the scan circuit (done in software).
The keyboard is shown in figure 2.8.

Buffer U50 (figure 2.7) is used to read the identity of the connected pod and to write clock and qualifier selection signals to the pod. The direction is controlled by means of signal PODDIR (comes from the microprocessor via PPI U15)
Buffer U64 is used to buffer some control signals for the pod:
  write signal for pod (BFPODWRT)
  pod select signals (BFPODSEL) which determine the pod mode
  internal sampling clock (BFCLKOUT)

These control signals will be described with the pod with which are used.

Clock generation

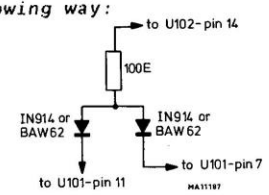
The internal sampling clock (100 MHz) is derived from a 50 MHz oscillator (U55). Transistor Q1 with tuned tank circuit L1, C4 and R3 filter the second hormonic out of this oscillator signal, which is then amplified by transistor Q2.

The 6.2016 MHz clock frequency for the microprocessor is generated by oscillator U23.
This 6.2016 MHz signal is also used as the dot clock for the video interface circuit.

NOTE: 1. For instruments that are connected to a 60 Hz mains, a second oscillator frequency is available (6.25 MHz), derived from the 50 MHz oscillator (via U54). This is to prevent magnetic mains influence on the CRT display. The selection between these two frequencies is done with the jumper near U23 (after the modification described below, this is not jumper selectable anymore!!). A second jumper (near L1) must be changed also to inform the microprocessor if it is a 60 Hz or a 50 Hz mains. The microprocessor can read the position of this jumper via U53. This is necessary for correct initialisation of the video interface (8276).

2. In some instruments, under some circumstances (sometimes after taking-in data with a 68000 microprocessor pod), dots and/or dashes appear random at the screen. This is caused by a bad termination of the 6.2016 MHz clock that goes to the video circuit. If you ever see this appearing, the following modifications have to be done:

- *Cut the track that goes to jumper J6, pin 38 (at the capture board).*
- *This instruction is different for the two different revisions of the capture board.*
  revision C: Cut-off pins of jumper JP2 (near U23).
  Add a wire between pins 2 and 3 of jumper JP2.
  revision B: Put the jumper near U23 in the "60 Hz position" (left).
- *On the solder side, add a wire (as short as possible) between U23-pin 8 and U110-pin 7 (near 8085 microprocessor).*
- *On the solder side, add a wire between U110-pin 1 and U110-pin 8.*
- *On the solder side, connnect a capacitor of 150 pF between pins 7 and 8 of U110.*
- *On the solder side, add a resistor and two diodes to U101/U102 (next to U110), in the following way:*



In instruments with a serial number 1850 or higher, these modifications are done standard.
Whenever you see a PM 3632 in your workshop, you should build-in these modifications.

The frequency of the internal clock (100 MHz) is affected by clock dividers U59, U60, U51 and U52, timer U16 (8155) and multiplexer U53.
These circuits form the internal sampling clock (CLKOUT) that goes to the pod via buffer U64 (BFCLKOUT).
Signal PSTOP takes care of a synchronous start and stop of the internal sampling clock CLKOUT. Signal PSTOP comes from the microprocessor via PPI U134.
The circuits that are used in the different clock ranges are listed in the table on the next page:

CLKOUT:	source:	via:
10ns	100 MHz (U62, U61)	direct, U63
20.....70 ns	100 MHz (U62, U61)	U59, U60, U53, U63
80ns.....9.9 us	20...70ns (U59, U60)	U51, U52, U53, U63
10us.....200 ms	40 ns, 50 ns> >(U51, U52)	Timer U16, U53, U63
	1 us, 12.5us>	

NOTE: U51, U52, U59, U60 are selected components. When changing these, only order the components listed in the spare parts list (see chapter 2.5).

Multiplexer U53 is set used to select the required path for the internal clock signal to form signal CLKOUT. This is done with clock selection signals CLKSEL0 and CLKSEL01 (come from the microprocessor via PPI U16).
Signals CNPRE 0...CNPRE 7 (counter preset) are used to load a certain value in the counters for correct division of the 100 MHz signal. These signals come from the microprocessor via PPI U136.
Signals PRESCAL0...PRESCAL3 (prescale) are used to set the modes for counters U59 and U560 (count up/down, shift left/right, hold) : These signals come from the microprocessor via PPI U16.

The internal sampling clock CLKOUT goes to the pod via buffer U64. In the pod itself the selection is made between internal or external clock. The selected clock comes back as signal SCLK02 (via U45, see figure 2.14) and is connected to U65 that sets the different clock signals for the input demultiplexers (signals SCLKP0...SCLKP3). This setting is done by means of signals SCPSEL (clock pulse select) and SCPEN (clock pulse enable).

LIST OF SIGNAL NAMES (diagram 2)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name. A ? indicates that the source cannot be defined (for example one signal-name can come from different pods, but only one can be connected). A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	2
A 8	Addressline 8	2	6,21,22,23
A 9	Addressline 9	2	6,21,22,23
A10	Addressline 10	2	1,6,21,22,23
A11	Addressline 11	2	1,6,21,22,23
A12	Addressline 12	2	1,3,6,21,22,23
A13	Addressline 13	2	1,6,21,22,23
A14	Addressline 14	2	1,6,21,22,23
A15	Addressline 15	2	1,6,21,22,23
AD0	Address/data line 0	2	1,3,6,21,22,23 BD
AD1	Address/data line 1	2	1,3,6,21,22,23 BD
AD2	Address/data line 2	2	1,3,6,21,22,23 BD
AD3	Address/data line 3	2	1,3,6,21,22,23 BD
AD4	Address/data line 4	2	1,3,6,21,22,23 BD
AD5	Address/data line 5	2	1,3,6,21,22,23 BD
AD6	Address/data line 6	2	1,3,6,21,22,23 BD
AD7	Address/data line 7	2	1,3,6,21,22,23 BD
ADRL00	Address counter load	2	1,5,6
ALE	Address latch enable	2	1,6,21,22,23
BPFREQ	Beep frequency	2	2
BRDY	Video buffer ready	2	2
CCLK	Character clock	2	2

LIST OF SIGNAL NAMES (diagram 2, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
CNPRE0	Counter preset 0	2	1,3,5,6
CNPRE1	Counter preset 1	2	1,3,5,6
CNPRE2	Counter preset 2	2	1,3,5,6
CNPRE3	Counter preset 3	2	1,3,5,6
CNPRE4	Counter preset 4	2	1,3,5,6
CNPRE5	Counter preset 5	2	1,3,5,6
CNPRE6	Counter preset 6	2	1,3,5,6
CNPRE7	Counter preset 7	2	1,3,5,6
EN62*	Enable 62 channel mode	2	1,3,5,6
GPA0	General purpose attribute 0	2	2
GPA1	General purpose attribute 1	2	2
HRTC	Horizontal retrace	2	1,6,7,8,9,31
IO/M*	Input,output/ memory	2	1,6,21,22,23
MODE 4*	4channel mode	2	1,5,6
MODE32*	32 channel mode	2	1,5,6
OPINT*	Option interrupt	21,22,23	2 ?
PODCS*	Chip select pod buffer	2	1,3,6
PSTART	Pushbutton START depressed	2	6
PSTOP*	Pushbutton STOP depressed	2	1,3,6
RAMCS0*	RAM chip select 0	2	2
RAMCS1*	RAM chip select 1	2	2
RAMCS2*	RAM chip select 2	2	2
RAMCS3*	RAM chip select 3	2	1,3,6
RAMCS4*	RAM chip select 4	2	1,3,6
RD*	Read signal	2	1,3,6,21,22,23
READY	Ready	21,22,23	2 ?
RESET OUT	Reset out signal	2	1,3,6,21,22,23
S0	Status line 0	2	1,6,21,22,23
S1	Status line 1	2	1,6,21,22,23
SC1	Suppess cursor 1	2	2
SCLKP0	Select clock pulse 0	2	3,5
SCLKP1	Select clock pulse 1	2	3,5
SCLKP2	Select clock pulse 2	2	3,5
SCLKP3	Select clock pulse	2	3,5
SCPEN*	Selected clock pulse enable	2	1,3,5,6
SCPSEL	Selected clock pulse select	2	1,3,6
SIDBIT	Serial input data, addresscounter	3	2
SIGSEL0	Demultiplexers signal select 0	2	1,5,6
SIGSEL1	Demultiplexers signal select 1	2	1,5,6
SIGSEL2	Demultiplexers signal select 2	2	1,5,6
SIGSEL3	Demultiplexers signal select 3	2	1,5,6
SMODE	Select mode	2	1,5,6
STATRAM0	Sequence controller RAM, bit 0	2	6
STATRAM1	Sequence controller RAM, bit 1	2	6
STATRAM2	Sequence controller RAM, bit 2	2	6
STATRAM3	Sequence controller RAM, bit 3	2	6
STATREN*	Sequence controller enable	2	6
STOP	Stop	6	2
STORE*	Store information	2	1,5,6
TAD8CLR*	Address counter, bit 8 clear	2	1,5,6
TAD8SET*	Address counter, bit 8 set	2	1,5,6
TAD9CLR*	Address counter, bit 9 clear	2	1,5,6
TAD9SET*	Address counter, bit 9 set	2	1,5,6
TIMCRSR	Timing cursors	2	2
TRACGAT0	Data qualification gate 0	2	2,6
TRACGAT1	Data qualification gate 1	2	2,6
TRACGAT2	Data qualification gate 2	2	2,6
TRACGAT3	Data qaulification gate 3	2	6
TRACTL0	Data qualification control line 0	2	6
TRACTL1	Data qualification control line 0	2	6
TRACWR*	Data aquisition memory write	2	1,5,6
TRGREN*	Trigger enable	2	1,5,6
TWA0	Triggerword A, RAM 0	2	1,6
TWA1	Triggerword A, RAM 1	2	1,6
TWA2	Triggerword A, RAM 2	2	1,6
TWA3	Triggerword A, RAM 3	2	1,6
TWB0	Triggerword B, RAM 0	2	1,6
TWB1	Triggerword B, RAM 1	2	1,6
TWB2	Triggerword B, RAM 2	2	1,6
TWB3	Triggerword B, RAM 3	2	1,6
TWC0	Triggerword C, RAM 0	2	1,6
TWC1	Triggerword C, RAM 1	2	1,6

LIST OF SIGNAL NAMES (diagram 2, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
TWC2	Triggerword C, RAM 2	2	1,6
TWC3	Triggerword C, RAM 3	2	1,6
TWD0	Triggerword D, RAM 0	2	1,6
TWD1	Triggerword D, RAM 1	2	1,6
TWD2	Triggerword D, RAM 2	2	1,6
TWD3	Triggerword D, RAM 3	2	1,6
VIDEO	Video signal	2	1,6,7,8,31
VIDLOAD*	Video load	2	2
VRTC	Vertical retrace	2	1,6,7,8,31
WR*	Write signal	2	1,2,3,6,21,22,23

LIST OF SIGNAL NAMES (diagram 3)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
100 MHz	Internal sampling clock source	3	3
6.2016 MHz	Video and uP clock	3	1,2,6,21,22,23
6.25 MHz	Video and uP clock	3	not used
A12	Addressline 12	2	3
AD0	Address/data line 0	2	3 BD
AD1	Address/data line 1	2	3 BD
AD2	Address/data line 2	2	3 BD
AD3	Address/data line 3	2	3 BD
AD4	Address/data line 4	2	3 BD
AD5	Address/data line 5	2	3 BD
AD6	Address/data line 6	2	3 BD
AD7	Address/data line 7	2	3 BD
ADROVR	Address counter overflow	5	3
BFCLKOUT	Buffered int. sampling clock, out	3	1,11,13
BFPODSEL0	Buffered pod select 0	3	1,11,13,16,18,19,20
BFPODSEL1	Buffered pod select 1	3	1,11,16,18,19,20
BFPODSEL2	Buffered pod select 2	3	1,11,16,18,19,20
BFPODWRT*	Buffered pod write	3	1,11,13,16,18,19,20
CLKOUT	Internal sampling clock, out	3	3
CLKSEL0	Internal sampling clock, select 0	3	3
CLKSEL1	Internal sampling clock, select 1	3	3
CNPRE0	Counter preset 0	2	3
CNPRE1	Counter preset 1	2	3
CNPRE2	Counter preset 2	2	3
CNPRE3	Counter preset 3	2	3
CNPRE4	Counter preset 4	2	3
CNPRE5	Counter preset 5	2	3
CNPRE6	Counter preset 6	2	3
CNPRE7	Counter preset 7	2	3
DELAY*	Final delay finished	3	1,6
DLYCLK	Final delay counter clock	6	3
EN62*	Enable 62 channel mode	2	3
OP0SEL*	Select option slot 0	3	1
OP1SEL*	Select option slot 1	3	1
OP2SEL*	Select option slot 2	3	1
OPSEL*	Option select; slot 0,1 or 2	3	21,22,23
POOCS*	Chip select pod buffer	2	3

LIST OF SIGNAL NAMES (diagram 3, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
PODDIR	Pod buffer direction	3	3
POOSEL0	Pod select 0	3	3
PODSEL1	Pod select 1	3	3
POOSEL2	Pod select 2	3	3
PODWRT*	Pod write	3	3
PRESCAL0	Preset sampling clock logic 0	3	3
PRESCAL1	Preset sampling clock logic 1	3	3
PRESCAL2	Preset sampling clock logic 2	3	3
PRESCAL3	Preset sampling clock logic 3	3	3
PSTOP*	Pushbutton STOP depressed	2	3
RAMCS3*	RAM chip select 3	2	3
RAMCS4*	RAM chip select 4	2	3
RD*	Read signal	2	3
RESET OUT	Reset out signal	2	3
SCLKØ2	Selected clock, phase 2	5	3
SCLKP0	Select clock pulse 0	2	3
SCLKP1	Select clock pulse 1	2	3
SCLKP2	Select clock pulse 2	2	3
SCLKP3	Select clock pulse	2	3
SCPEN*	Selected clock pulse enable	2	3
SCPSEL	Selected clock pulse select	2	3
SIOBIT	Serial input data, addresscounter	3	1,2,6
SIG24	Input channel 24	11,13,16,18 19,20	3 BD
SI625	Input channel 25	11,13,16,18 19,20	3 BD
SI626	Input channel 26	11,13,16,18 19,20	3 BD
SI627	Input channel 27	11,13,16,18 19,20	3 BD
SI628	Input channel 28	11,13,16,18 19,20	3 BD
SI629	Input channel 29	11,13,16,18 19,20	3 BD
SI630	Input channel 30	11,13,16,18 19,20	3 BD
SI631	Input channel 31	11,13,16,18 19,20	3 BD
TADR8	Address counter bit 8	5	3
TADR9	Address counter bit 9	5	3
TRCD 0	Acquisition data, ch. 0	5	3
TRCD 1	Acquisition data, ch. 1	5	3
TRCD 2	Acquisition data, ch. 2	5	3
TRCD 4	Acquisition data, ch. 4	5	3
TRCD 5	Acquisition data, ch. 5	5	3
TRCD 6	Acquisition data, ch. 6	5	3
TRCD 7	Acquisition data, ch. 7	5	3
TRCD 8	Acquisition data, ch. 8	5	3
TRCD 9	Acquisition data, ch. 9	5	3
TRCD10	Acquisition data, ch. 10	5	3
TRCD11	Acquisition data, ch. 11	5	3
TRCD12	Acquisition data, ch. 12	5	3
TRCD13	Acquisition data, ch. 13	5	3
TRCD14	Acquisition data, ch. 14	5	3
TRCD15	Acquisition data, ch. 15	5	3
TRCD16	Acquisition data, ch. 16	5	3
TRCD17	Acquisition data, ch. 17	5	3
TRCD18	Acquisition data, ch. 18	5	3
TRCD19	Acquisition data, ch. 19	5	3
TRCD20	Acquisition data, ch. 20	5	3
TRCD21	Acquisition data, ch. 21	5	3
TRCD22	Acquisition data, ch. 22	5	3
TRCD23	Acquisition data, ch. 23	5	3
TRCD24	Acquisition data, ch. 24	5	3
TRCD25	Acquisition data, ch. 25	5	3
TRCD26	Acquisition data, ch. 26	5	3
TRCD27	Acquisition data, ch. 27	5	3
TRCD28	Acquisition data, ch. 28	5	3
TRCD29	Acquisition data, ch. 29	5	3
TRCD30	Acquisition data, ch. 30	5	3
TRCD31	Acquisition data, ch. 31	5	3
WR*	Write signal	2	3

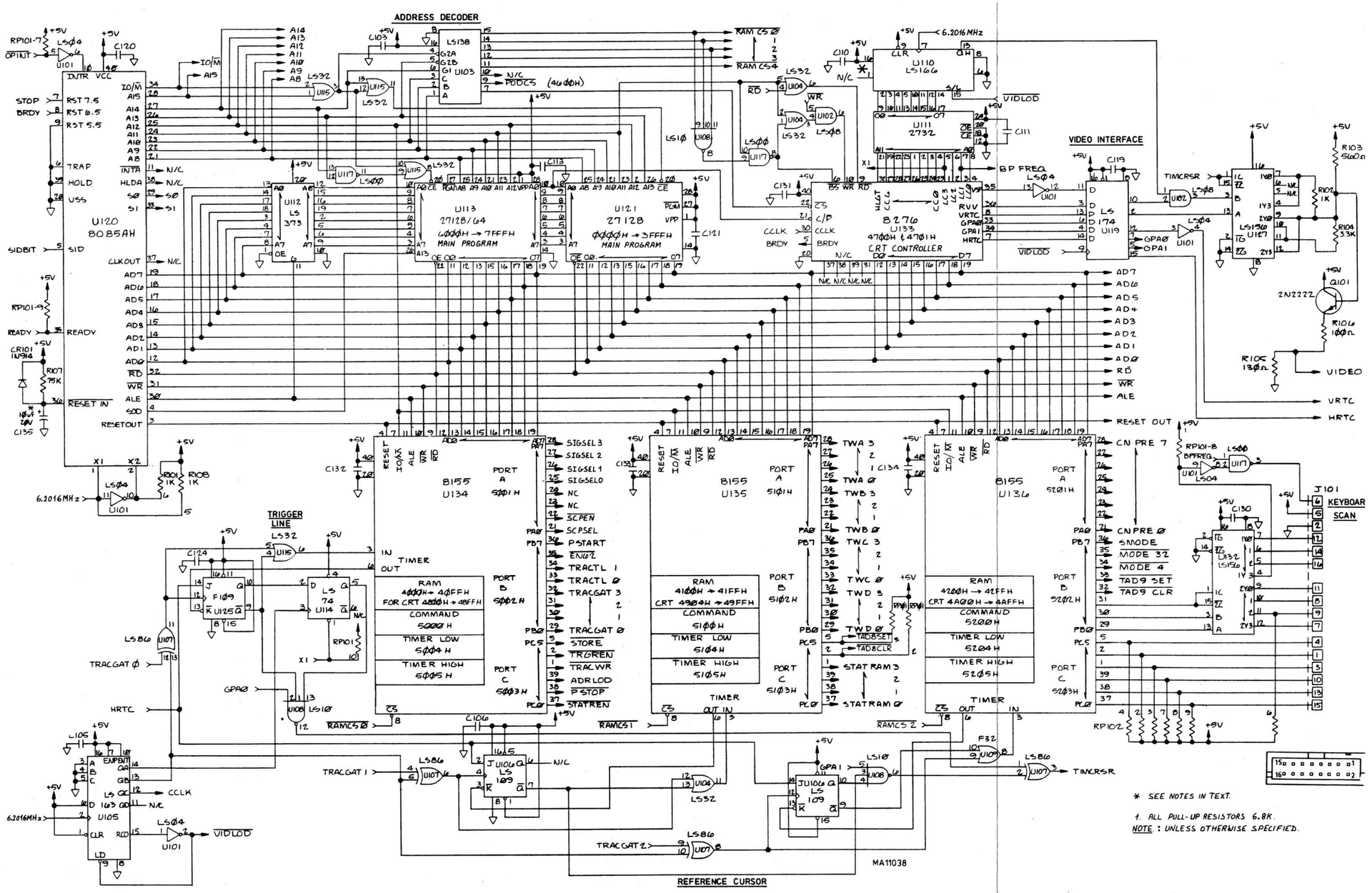


Figure 2.6 : Capture board, microcomputer (2).

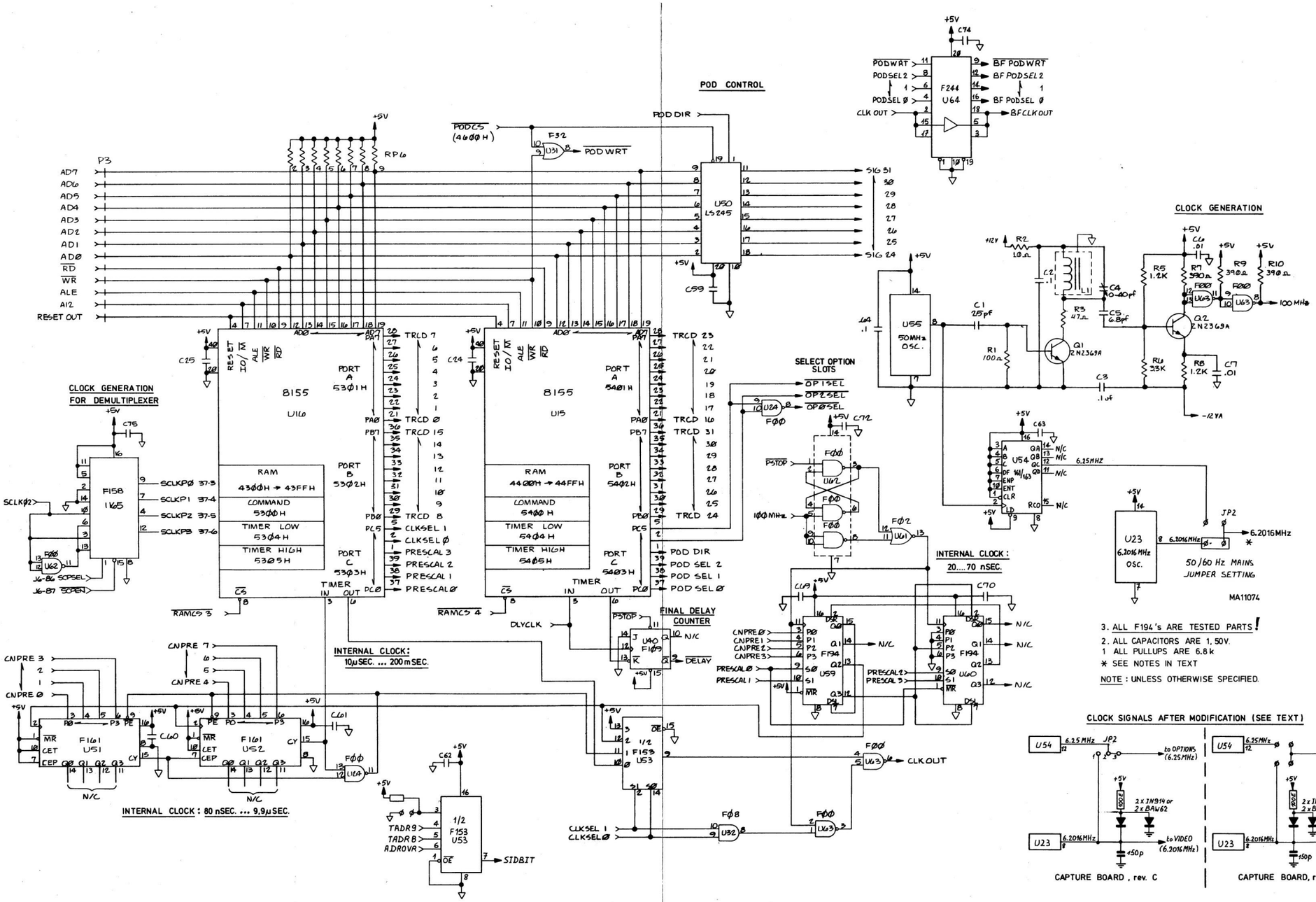


Figure 2.7 : Capture board, microcomputer clock generation (3).

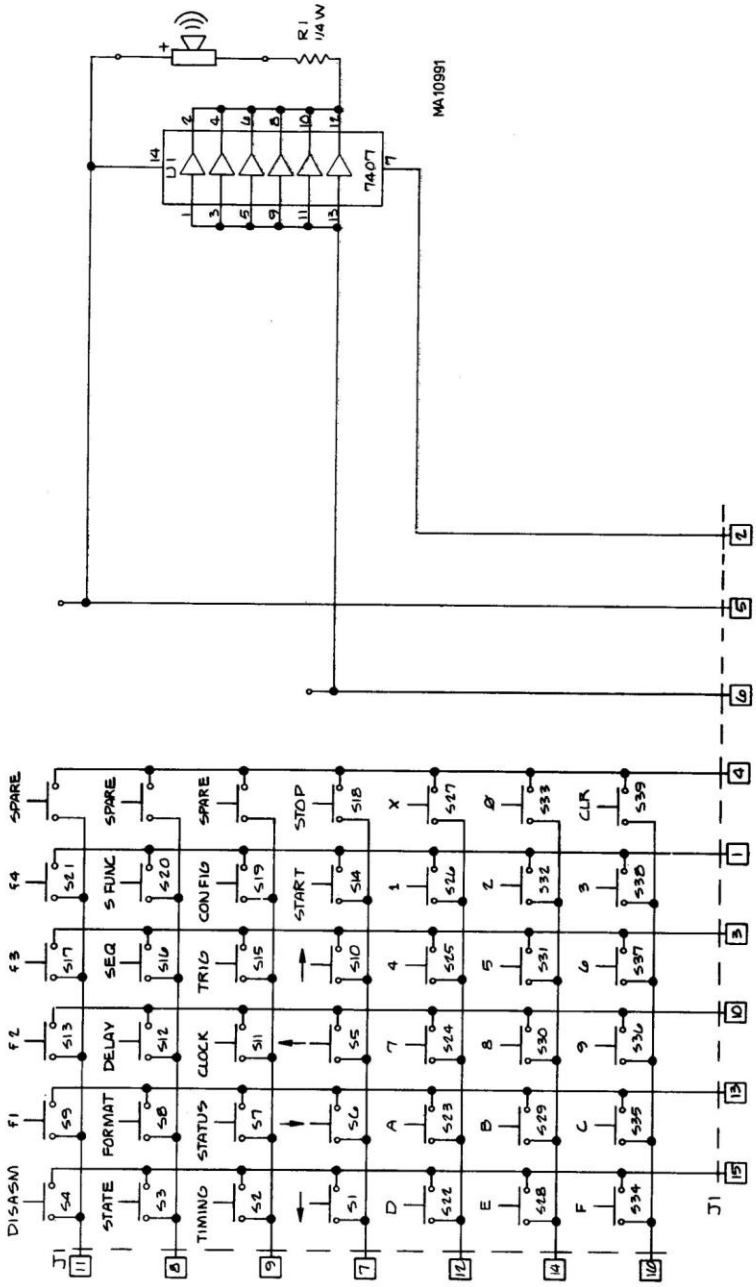


Figure 2.8 : PM 3632, keyboard (4).

2.2.2 INPUT DEMULTIPLEXERS

Data from the pod (SIG0...SIG31) is first processed by the input demultiplexers which organizes it into 32-bit words which can be handled by the PM 3632 circircuitry.
Its four modes accept data in word widths of 4, 8, 16, and 32 bits. Input rates in the 4-bit mode are up to 100 MHz. The maximum rate decreases in a binary fashion to 12.5 MHz at 32 bits.

Clocks for the input registers and buffers are developed by U37 and U45 (see upper left part of figure 2.14). U45 operates as a slave, duplicates the signals of U37. This allows driving more loads than U37 could by itself.
SMODE drives Pin 10 of U37-U49; this signal is set by the microprocessor and determines the mode in which U37 operates (load or shift right).
SCLKP 0-3 are also set by the microprocessor and determine the preload of the shift register before its clock is enabled. These signals are also modified by U65 (see figure 2.7) in the 8-bit mode (via signal SCLK02).
SCLK is the clock signal coming from the pod, and can be supplied by the external or internal clock (switching is done in the pod).
Signal QUALIN (qualifier signal from pod) inhibits the clock signals for the demultiplexers as long as the qualifier condition is nut met.
In the 4-bit mode, a pair of adjecent ones is shifted continuously through the the register, providing for four 25 MHz clocks skewed from each other by 90 degrees.
In other widths, the outputs are clocked back into the inputs of the register via U65, producing four clocks in one or two phases. These clocks clock the eight 74F399s, as described below (for timing relations of the clock generation, refer also to figure 2.9).

In each of the four modes U13, U14, U21, U22, U29, U30, U38 and U46 register the data directly from the pod.
The modes are controlled with SIGSEL0...SIGSEL3 signal select from the microprocessor.
In the 4-bit mode, the MUX select lines (SIGSEL0...SIGSEL3) are set to cause U14, U22, U30 and U38 to capture the data on lines SIG0...SIG3.
U13, U21, U29 and U46 capture the output of the first registers, and are each clocked at the same time as their predecessor (see also figure 2.9; only the data flow for channel 0 is described).

As an example, U38 is clocked to collect SIG0...SIG3 at every forth sample time. At the same time, U46 is loaded with the output of U38, which is the forth oldest sample.
Every eight samples, this data is loaded into the output register composed of U12, U20, U28 and U43 (by means of signals MREGCK and MREGEN*:12,5 MHz max.)
In 4 bit mode the outputs of U38 and U46 are latched at an intermediate time (4th sample) to insure proper hold time for the ouput registers (signal MODE4*).

In 32-bit and 16-bit mode, all registers are clocked at the same time.
The 16-bit operation is achieved by cascading the pairs, as in 4-bit mode (refer to figures 2.10 and 2.11).
The 8-bit mode is like the 4-bit mode, except the registers are clocked four at a time instead of two at a time (refer to figure 2.12).

For 16-bit microprocessor pods, more than 32 channels are required.
Therefore there is also a 62 bit mode which is for the input demultiplexers the same as the 32 bit mode. In this case bit 31 (signal FRAME 62; is used as control signal for the trigger circuits).
The control signals, for the input demultiplexers, for the different modes are listed in the table in figure 2.14).

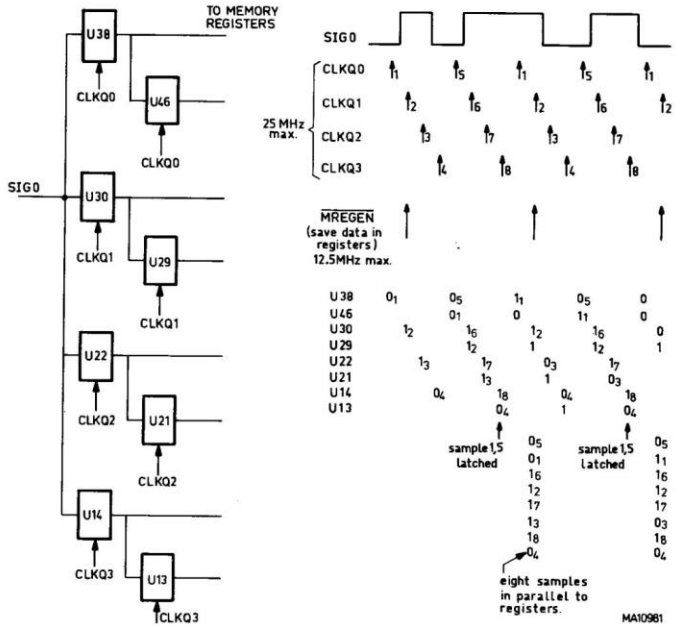


Figure 2.9 : 100 MHz sampling.

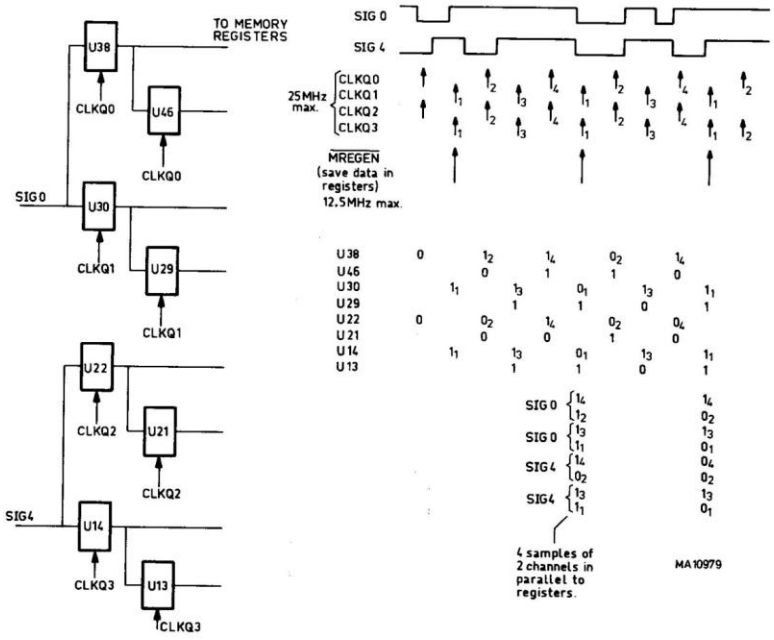


Figure 2.10 : 50 MHz sampling.

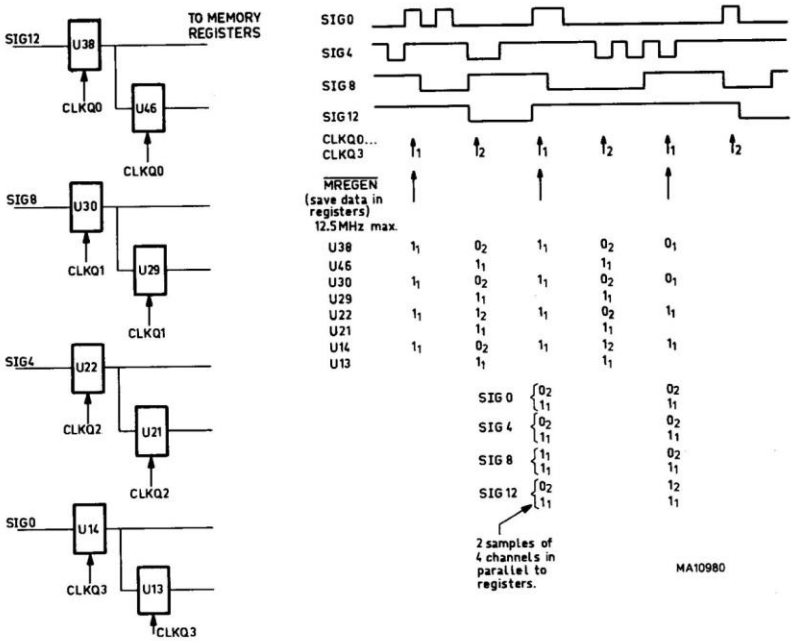


Figure 2.11 : 25 MHz sampling

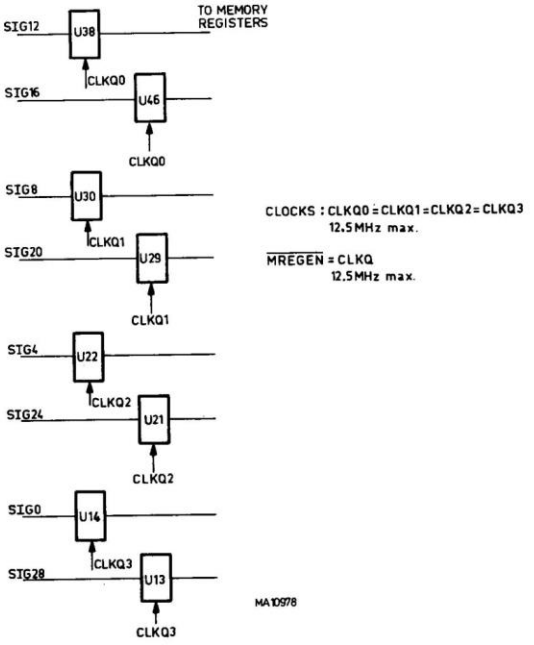


Figure 2.12 : 12.5 MHz sampling

2.2.3 DATA ACQUISITION MEMORIES

U58, U56, and the delay line (U57) form the clock for the data acquisition memory (see figure 2.14). Also the clock for the trigger circuits is generated here (TRGCLK).
U1...U8 form the data acquisition RAMs.
These 4-bit-by-1024-word memories store a total of 32k bits.
U41, U42 (8 address lines) and U39 form the address counter for these RAMs.
Each time a 32-bit record is ready from the input demultiplexers (U43, etc.), U56 (pin 10) clocks this counter and causes a write operation. U40 detects address overflow (signal ADROVR) of the address counter, which does not occur for a small numbers of clocks (those which are less than one memory full).
The overflow only occurs after the trigger condition is fullfilled (signal TRCCNTEN; trace count enable), and the memory is full. Otherwise this counter continues to roll over repetitively until a trigger condition is encountered.
The microprocessor can read signal ADROVR via its serial input (via U53, see figure 2.7); this is necessary for correct data reconstruction.
Signals CNPRE0...CNPRE7 (counter preset) TAD8SET, TAD8CCR, TAD9SET, TAD9CLR and ADRLOD (address load) are used to address the data acquisition RAMs when the microprocessor wants to read the contents of the RAMs after data acquisition has stopped.
The I/O busses TRCD0...TRCD31 from these RAMs are also connected to U15 and U16 (PPIs, see figure 2.7) so that the microprocessor can read out the contents of this RAM.

2.2.4 TRIGGER AND SEQUENCE CIRCUITRY

U9, U17, U25 and U33 are the trigger RAMs (see figure 2.14).
In all modes except 32- and 62-bit, its address lines are driven by the same data as the data lines of the data acquisition RAMs (TRCD0...TRCD31 via MUXes).
In 32-bit and 62-bit mode, these signals are taken directly from the input registers of the input demultiplexer. Signal MODE32 selects the multiplexer inputs (U10, U11 etc).
Only in these two modes data qualification is possible.
The trigger RAM is loaded with the correct pattern by the microprocessor just prior to the start of recording (signal STORE).
If a data sample (used as address lines for the trigger RAMs) corresponds with a selected triggerword, the coresponding outputs of the RAMs will be active.
These outputs are logically "anded" or "ored", as required by U129 and U130 (see figure 2.15).
In 4, 8, 16 and 32 bit modes, only 1/4 of the trigger RAMs is used.
A second quarter is used in 32 bit mode for state qualification: In that case the enable word and disable word are both located at the position of triggerword 0, while TRCSTAT (trigger control state) does the switching between the two quarters (see also figure 2.13).
The second half of the RAMs is used in 62 bit mode.
The 62 bit mode is used when a 16-bit microprocessor pod is connected to the logic analyzer. These pods divide a maximum of 62 input channels in two frames of 31 bits (signal FRAME62 indicates which half is currently in the analyzer).
For triggering on the second half of the 62 bit triggerword, the triggerram is switched-over to the second half (signal FRAME62, see also fig. 2.13).
Signal TRGEN (trigger enable) is used to enable triggering after the correct pattern is loaded in the RAMs.

2.2.5 SEQUENCE CONTROLLER

Sequence controller.

The outputs of U129 and U130 are processed by the sequence controller.
U131 is the input register for this machine, and directly drives U124, the sequence controller RAM.
This RAM is loaded by the microprocessor with a program corresponding to the selected sequence. Its output is registered by U122.
Four lines are used as a feedback to the RAM; These lines indicate the state in which the controller currently is (2 states for initialisation, 13 are left for user defined sequences; state 15 is stop)
U123 decodes the trigger condition state 15 and starts the delay counter composed of U126 and the timer portion of U15 (see figure 2.7). When the delay has expired, U114 is set (stop becomes active which stops the clock generation).
Pressing the STOP pushbutten forces the sequence controller to the stop condition (via U123) via signal PSTOP* (from the microprocessor).

Data qualification.

The state and combinational qualification circuit is formed by U116, U125, U118 and associated components.
Signals TRACGAT0...TRACGAT3 select the words for state or comb. qualification.

Due to the hardware connection (U116), data qualification in 62-bit mode is only possible on the first 31-bit half of the incoming data. This, because in the second half of the data, the triggerrams are also switched-over to the second half.
Allowing data qualification on the second half of the data **could** result in qualifying one half of the capture data, and disqualifying the other half!
Therefore, only data qualification on the first half is allowed (by the software). Qualification of this half however also qualifies the second. Also disqualification of the first half will disqualify thee second half (signal 0F62 holds signal TRCCNTEN stable for two halfs).

Comb. qualification

-only : When the qualified word is found U116 ouputs a "zero" which makes TRCCNTEN (trace counter enable) "zero" via U118. This signal enables the address counter for the data acquisition memories to increment. In this way the qualified word is stored in memory.

-all but: Signal TRCCNTEN will be "zero" (via U118) until a qualified word is found (via U116). This qualified word makes signal TRCCNTEN "high" via U125 and U118. The address counter will not increment now, so the qualified word will be overwritten by the next word.

Signals TRACTL0 and TRACTL1 set multiplexer U118 to input 0 for the "all but mode" or input 1, for the "only" mode.

State qualification

When the enable word is found in the trigger RAMs (stored at the position of word 0) it passes U116 (in the first quarter of these memories).
This causes signal TRCCNTEN to go to "zero" via U118 (input 3). Now the address counter for the data acquisition RAMs is enabled and data will be stored in A memory.

The enable word also toggles JK flip flop U125. Now signal TRCSTAT (trigger control state) switches the trigger RAMs to the second quarter. These RAMs will now start searching for the disable word (stored at the position of word 0). When the disable word is found signal TRCCNTEN will go "high" again which disables the address counter for the data acquisition RAMs.
Signal TRCSTAT switches the trigger RAMs to the first quarter again to search for the enable word again.
Signal LASTGAT is formed via register U122 and is used to hold signal TRCSTAT to the level that it is just set to by the enable or disable word (via U109), until the next qualified word appears.

In 62 bit mode signal DF62 (via U122) holds signal TRCSTAT to the just set level until the next qualified word appears. In this case, state qualification is only possible on the first 31 bit frame of the 62 bit word.

Only qualified words should be able to increment the final delay counter. This is done via U118 output 5 which enables the clock for the delay counter (via U122, U109), however this is done one clockpulse later than the one that belonged to the qualified word. Therefore the last qualified word will not increment the delay counter.
The enabling of a final clockpulse for the delay counter is now done via the feedback of the "enable pin" pin 3 of U137. This enables one more clockpulse (via U118 pin 5); that stops the final delay counter.

2.2.6 OPTION CARD INTERFACE

The three connectors provided on the Capture Board for option expansion are a direct expansion of the microprocessor bus, with the exception of OPINT* and OPSEL* (see figure 2.4, J3, J4 and J5).
OPINT is buffered and applied directly to the interrupt line of the processor.

This signal is "wire-ored".
OP?SEL is the option card select line.
There are three option select lines (?=1, 2, and 3), generated by U15 (see figure 2.7)
Each option card is enabled when its option select line is low; it then provides overlay RAM, ROM, and/or I/O as required (see also figure 2.5; memory map).

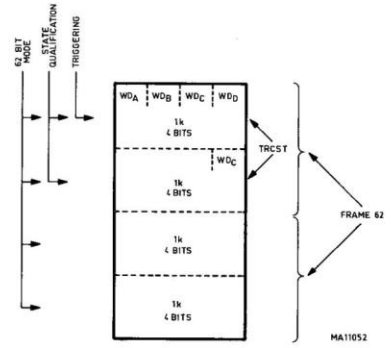


Figure 2.13: Trigger ram.

LIST OF SIGNAL NAMES (diagram 5)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
ADRL00	Address counter load	2	5
ADROVR	Address counter overflow	5	3
CNPRE0	Counter preset 0	2	5
CNPRE1	Counter preset 1	2	5
CNPRE2	Counter preset 2	2	5
CNPRE3	Counter preset 3	2	5
CNPRE4	Counter preset 4	2	5
CNPRE5	Counter preset 5	2	5
CNPRE6	Counter preset 6	2	5
CNPRE7	Counter preset 7	2	5
EN62*	Enable 62 channel mode	2	5
FRAME62	62 channel mode, frame indication	5	1,5,6
M32T 2	32 channel mode, trigger data 2	5	5
M32T 3	32 channel mode, trigger data 3	5	5
M32T 4	32 channel mode, trigger data 4	5	5
M32T 5	32 channel mode, trigger data 5	5	5
M32T 6	32 channel mode, trigger data 6	5	5
M32T 7	32 channel mode, trigger data 7	5	5
M32T 8	32 channel mode, trigger data 8	5	5
M32T 9	32 channel mode, trigger data 9	5	5
M32T 0	32 channel mode, trigger data 0	5	5
M32T 1	32 channel mode, trigger data 1	5	5
M32T10	32 channel mode, trigger data 10	5	5
M32T11	32 channel mode, trigger data 11	5	5
M32T12	32 channel mode, trigger data 12	5	5
M32T13	32 channel mode, trigger data 13	5	5
M32T14	32 channel mode, trigger data 14	5	5
M32T15	32 channel mode, trigger data 15	5	5
M32T16	32 channel mode, trigger data 16	5	5
M32T17	32 channel mode, trigger data 17	5	5
M32T18	32 channel mode, trigger data 18	5	5
M32T19	32 channel mode, trigger data 19	5	5
M32T20	32 channel mode, trigger data 20	5	5
M32T21	32 channel mode, trigger data 21	5	5
M32T22	32 channel mode, trigger data 22	5	5
M32T23	32 channel mode, trigger data 23	5	5
M32T24	32 channel mode, trigger data 24	5	5
M32T25	32 channel mode, trigger data 25	5	5
M32T26	32 channel mode, trigger data 26	5	5
M32T27	32 channel mode, trigger data 27	5	5
M32T28	32 channel mode, trigger data 28	5	5
M32T29	32 channel mode, trigger data 29	5	5
M32T30	32 channel mode, trigger data 30	5	5
M32T31	32 channel mode, trigger data 31	5	5
MODE 4*	4channel mode	2	5
MODE32	32 channel mode	5	5
MODE32*	32 channel mode	2	5
MREGCK	Memory register clock	5	5
MREGEN*	Memory register enable	5	5
QUALIN	Qualifier in signal	10,13,16,18 19,20	5 ?
SCLK	Selected clock	11,13,16,18 19,20	5 ?
SCLKØ2	Selected clock, phase 2	5	3

LIST OF SIGNAL NAMES (diagram 5, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
SCLKP0	Select clock pulse 0	2	5	
SCLKP1	Select clock pulse 1	2	5	
SCLKP2	Select clock pulse 2	2	5	
SCLKP3	Select clock pulse	2	5	
SCPEN*	Selected clock pulse enable	2	5	
SIG 0	Input channel 0	10,12,16,18 19,20	5	?
SIG 1	Input channel 1	10,12,16,18 19,20	5	?
SIG 2	Input channel 2	10,12,16,18 19,20	5	?
SIG 3	Input channel 3	10,12,16,18 19,20	5	?
SIG 4	Input channel 4	10,16,18,19 20	5	?
SIG 5	Input channel 5	10,16,18,19 20	5	?
SIG 6	Input channel 6	10,16,18,19 20	5	?
SIG 7	Input channel 7	10,16,18,19 20	5	?
SIG 8	Input channel 8	10,16,18,19 20	5	?
SIG 9	Input channel 9	10,16,18,19 20	5	?
SIG10	Input channel 10	10,16,18,19 20	5	?
SIG11	Input channel 11	10,16,18,19 20	5	?
SIG12	Input channel 12	10,16,18,19 20	5	?
SIG13	Input channel 13	10,16,18,19 20	5	?
SIG14	Input channel 14	10,16,18,19 20	5	?
SIG15	Input channel 15	10,16,18,19 20	5	?
SIG16	Input channel 16	11,16,18,19 20	5	?
SIG17	Input channel 17	11,16,18,19 20	5	?
SIG18	Input channel 18	11,16,18,19 20	5	?
SIG19	Input channel 19	11,16,18,19 20	5	?
SIG20	Input channel 20	11,16,18,19 20	5	?
SIG21	Input channel 21	11,16,18,19 20	5	?
SIG22	Input channel 22	11,16,18,19 20	5	?
SIG23	Input channel 23	11,16,18,19 20	5	?
SIG24	Input channel 24	11,13,16,18 19,20	5	? BD
SIG25	Input channel 25	11,13,16,18 19,20	5	? BD
SIG26	Input channel 26	11,13,16,18 19,20	5	? BD
SIG27	Input channel 27	11,13,16,18 19,20	5	? BD
SIG28	Input channel 28	11,13,16,18 19,20	5	? BD
SIG29	Input channel 29	11,13,16,18 19,20	5	? BD
SIG30	Input channel 30	11,13,16,18 19,20	5	? BD
SIG31	Input channel 31	11,13,16,18 19,20	5	? BD
SIGSEL0	Demultiplexers signal select 0	2	5	

LIST OF SIGNAL NAMES (diagram 5, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SIGSEL1	Demultiplexers signal select 1	2	5
SIGSEL2	Demultiplexers signal select 2	2	5
SIGSEL3	Demultiplexers signal select 3	2	5
SMODE	Select mode	2	5
STOP*	Stop	6	5
STORE*	Store information	2	5
TA08CLR*	Address counter, bit 8 clear	2	5
TA08SET*	Address counter, bit 8 set	2	5
TA09CLR*	Address counter, bit 9 clear	2	5
TA09SET*	Address counter, bit 9 set	2	5
TAQR8	Address counter bit 8	5	3
TAQR9	Address counter bit 9	5	3
TRACWR*	Data aquisition memory write	2	5
TRCCNTEN	Address counter enable	6	5
TRCQ 0	Acquisition data, ch. 0	5	3
TRCQ 1	Acquisition data, ch. 1	5	3
TRCQ 2	Acquisition data, ch. 2	5	3
TRCQ 4	Acquisition data, ch. 4	5	3
TRCQ 5	Acquisition data, ch. 5	5	3
TRCQ 6	Acquisition data, ch. 6	5	3
TRCQ 7	Acquisition data, ch. 7	5	3
TRCQ 8	Acquisition data, ch. 8	5	3
TRCQ 9	Acquisition data, ch. 9	5	3
TRCQ10	Acquisition data, ch. 10	5	3
TRCQ11	Acquisition data, ch. 11	5	3
TRCQ12	Acquisition data, ch. 12	5	3
TRCQ13	Acquisition data, ch. 13	5	3
TRCQ14	Acquisition data, ch. 14	5	3
TRCQ15	Acquisition data, ch. 15	5	3
TRCQ16	Acquisition data, ch. 16	5	3
TRCQ17	Acquisition data, ch. 17	5	3
TRCQ18	Acquisition data, ch. 18	5	3
TRCQ19	Acquisition data, ch. 19	5	3
TRCQ20	Acquisition data, ch. 20	5	3
TRCQ21	Acquisition data, ch. 21	5	3
TRCQ22	Acquisition data, ch. 22	5	3
TRCQ23	Acquisition data, ch. 23	5	3
TRCQ24	Acquisition data, ch. 24	5	3
TRCQ25	Acquisition data, ch. 25	5	3
TRCQ26	Acquisition data, ch. 26	5	3
TRCQ27	Acquisition data, ch. 27	5	3
TRCQ28	Acquisition data, ch. 28	5	3
TRCQ29	Acquisition data, ch. 29	5	3
TRCQ30	Acquisition data, ch. 30	5	3
TRCQ31	Acquisition data, ch. 31	5	3
TRCSTAT	Data qualification trigger switch	6	5
TRG 4	Trigger data, channel 4	5	5
TRG 5	Trigger data, channel 5	5	5
TRG 6	Trigger data, channel 6	5	5
TRG 7	Trigger data, channel 7	5	5
TRG12	Trigger data, channel 12	5	5
TRG13	Trigger data, channel 13	5	5
TRG14	Trigger data, channel 14	5	5
TRG15	Trigger data, channel 15	5	5
TRG16	Trigger data, channel 16	5	5
TRG17	Trigger data, channel 17	5	5
TRG18	Trigger data, channel 18	5	5
TRG19	Trigger data, channel 19	5	5
TRG24	Trigger data, channel 24	5	5
TRG25	Trigger data, channel 25	5	5
TRG26	Trigger data, channel 26	5	5
TRG27	Trigger data, channel 27	5	5
TRGCLK	Trigger clock	5	1,6
TRGREN*	Trigger enable	2	5
TWA0	Triggerword A, RAM 0	5	1,6
TWA1	Triggerword A, RAM 1	5	1,6
TWA2	Triggerword A, RAM 2	5	1,6
TWA3	Triggerword A, RAM 3	5	1,6
TWB0	Triggerword B, RAM 0	5	1,6

LIST OF SIGNAL NAMES (diagram 5, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
TWB1	Triggerword B, RAM 1	5	1,6
TWB2	Triggerword B, RAM 2	5	1,6
TWB3	Triggerword B, RAM 3	5	1,6
TWC0	Triggerword C, RAM 0	5	1,6
TWC1	Triggerword C, RAM 1	5	1,6
TWC2	Triggerword C, RAM 2	5	1,6
TWC3	Triggerword C, RAM 3	5	1,6
TWD0	Triggerword D, RAM 0	5	1,6
TWD1	Triggerword D, RAM 1	5	1,6
TWD2	Triggerword D, RAM 2	5	1,6
TWD3	Triggerword D, RAM 3	5	1,6

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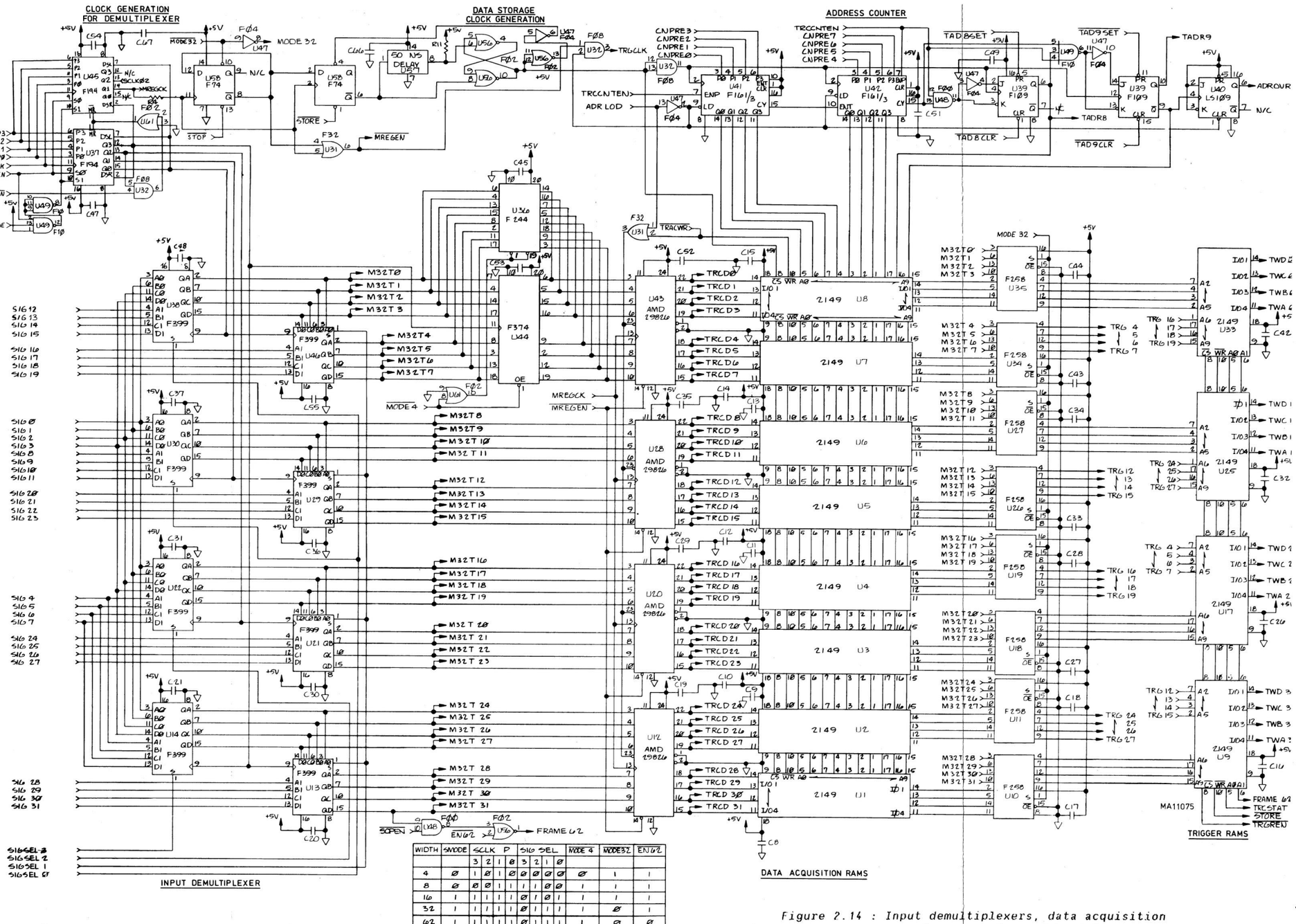


Figure 2.14 : Input demultiplexers, data acquisition memories and trigger RAMs (5)

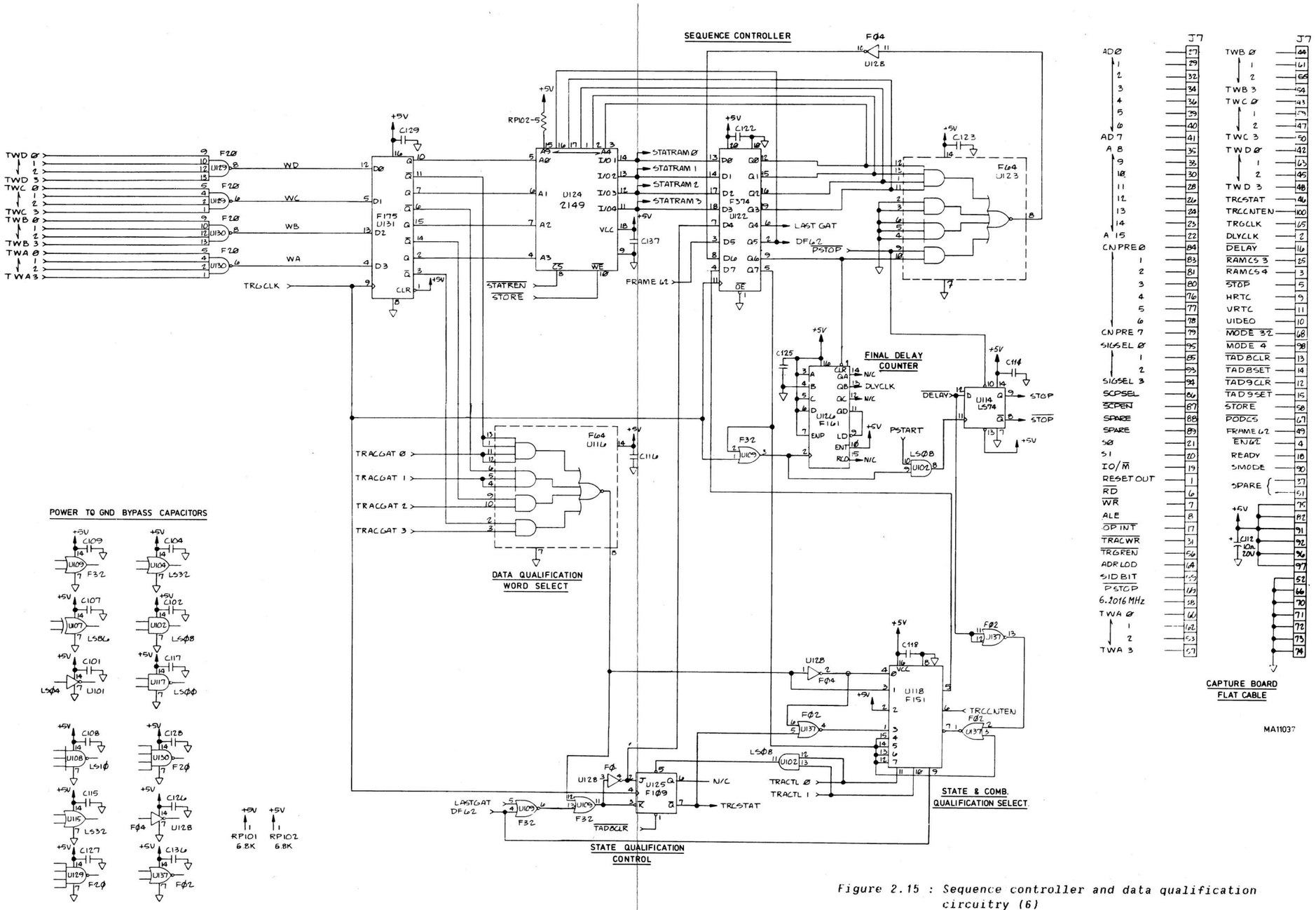


Figure 2.15 : Sequence controller and data qualification circuitry (6)

LIST OF SIGNAL NAMES (diagram 6)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	6
A 8	Addressline 8	2	6
A 9	Addressline 9	2	6
A10	Addressline 10	2	6
A11	Addressline 11	2	6
A12	Addressline 12	2	6
A13	Addressline 13	2	6
A14	Addressline 14	2	6
A15	Addressline 15	2	6
AD0	Address/data line 0	2	6 BD
AD1	Address/data line 1	2	6 BD
AD2	Address/data line 2	2	6 BD
AD3	Address/data line 3	2	6 BD
AD4	Address/data line 4	2	6 BD
AD5	Address/data line 5	2	6 BD
AD6	Address/data line 6	2	6 BD
AD7	Address/data line 7	2	6 BD
ADRLOD	Address counter load	2	6
ALE	Address latch enable	2	6
CNPRE0	Counter preset 0	2	6
CNPRE1	Counter preset 1	2	6
CNPRE2	Counter preset 2	2	6
CNPRE3	Counter preset 3	2	6
CNPRE4	Counter preset 4	2	6
CNPRE5	Counter preset 5	2	6
CNPRE6	Counter preset 6	2	6
CNPRE7	Counter preset 7	2	6
DELAY*	Final delay finished	3	6
DF62	Delayed frame indication	6	6
DLYCLK	Final delay counter clock	6	1,3,6
EN62*	Enable 62 channel mode	2	6
FRAME62	62 channel mode, frame indication	5	6
HRTC	Horizontal retrace	2	6
IO/M*	Input,output/ memory	2	6
LASTGAT	Last captured qualification word	6	6
MODE 4*	4channel mode	2	6
MODE32*	32 channel mode	2	6
OPINT*	Option interrupt	21,22,23	6 ?
P00CS*	Chip select pod buffer	2	6
PSTART	Pushbutton START depressed	2	6
PSTOP*	Pushbutton STOP depressed	2	6
RAMCS3*	RAM chip select 3	2	6
RAMCS4*	RAM chip select 4	2	6
RD*	Read signal	2	6
READY	Ready	21,22,23	6
RESET OUT	Reset out signal	2	6
S0	Status line 0	2	6
S1	Status line 1	2	6
SCPEN*	Selected clock pulse enable	2	6
SCPSEL	Selected clock pulse select	2	6
SIOBIT	Serial input data, addresscounter	3	6
SIGSEL0	Demultiplexers signal select 0	2	6
SIGSEL1	Demultiplexers signal select 1	2	6

LIST OF SIGNAL NAMES (diagram 6, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SIGSEL2	Demultiplexers signal select 2	2	6
SIGSEL3	Demultiplexers signal select 3	2	6
SMODE	Select mode	2	6
STATRAM0	Sequence controller RAM, bit 0	2	6
STATRAM1	Sequence controller RAM, bit 1	2	6
STATRAM2	Sequence controller RAM, bit 2	2	6
STATRAM3	Sequence controller RAM, bit 3	2	6
STATREN*	Sequence controller enable	2	6
STOP	Stop	6	1,2
STOP*	Stop	6	5,6
STORE*	Store information	2	6
TAD8CLR*	Address counter, bit 8 clear	2	6
TAD8SET*	Address counter, bit 8 set	2	6
TAD9CLR*	Address counter, bit 9 clear	2	6
TAD9SET*	Address counter, bit 9 set	2	6
TRACGAT0	Data qualification gate 0	2	6
TRACGAT1	Data qualification gate 1	2	6
TRACGAT2	Data qualification gate 2	2	6
TRACGAT3	Data qaulification gate 3	2	6
TRACTL0	Data qualification control line 0	2	6
TRACTL1	Data qualification control line 0	2	6
TRACWR*	Data aquisition memory write	2	6
TRCCNTEN	Address counter enable	6	1,5,6
TRCSTAT	Data qualification trigger switch	6	1,5,6
TRGCLK	Trigger clock	5	6
TRGREN*	Trigger enable	2	6
TWA0	Triggerword A, RAM 0	2,5	6 ?
TWA1	Triggerword A, RAM 1	2,5	6 ?
TWA2	Triggerword A, RAM 2	2,5	6 ?
TWA3	Triggerword A, RAM 3	2,5	6 ?
TWB0	Triggerword B, RAM 0	2,5	6 ?
TWB1	Triggerword B, RAM 1	2,5	6 ?
TWB2	Triggerword B, RAM 2	2,5	6 ?
TWB3	Triggerword B, RAM 3	2,5	6 ?
TWC0	Triggerword C, RAM 0	2,5	6 ?
TWC1	Triggerword C, RAM 1	2,5	6 ?
TWC2	Triggerword C, RAM 2	2,5	6 ?
TWC3	Triggerword C, RAM 3	2,5	6 ?
TWD0	Triggerword D, RAM 0	2,5	6 ?
TWD1	Triggerword D, RAM 1	2,5	6 ?
TWD2	Triggerword D, RAM 2	2,5	6 ?
TWD3	Triggerword D, RAM 3	2,5	6 ?
VIDEO	Video signal	2	6
VRTC	Vertical retrace	2	6
WR*	Write signal	2	6

2.3 VIDEO DISPLAY

The video display unit which is used in the PM 3632 is a 5 inch video display unit.
Input signals for the monitor are the HTRC (horizontal retrace), VRTC (vertical retrace) and VIDEO signals.

Because three versions are in the field, three circuit diagrams are enclosed, but it is not recommended to repair this unit because of the low price. Therefore a circuit description in not in this manual.

For those however who want to repair this unit we think these circuit diagrams are self-explanatory (the spare parts list in the back of this chapter contains Philips replacement parts for a few of the semiconductors used in the CRT's).

NOTE: The three different CRT units can be identified as follows:
CRT 1: Manufacturer, KAGA : shorter picture tube: type KT5SB31G-OS
CRT 2: Manufacturer, MOTOROLA : longer picture tube (almost reaches the power supply boards): type MD1000-390
CRT 3: Manufacturer, AUDIOTRONIX : short picture tube: type 946-48

LIST OF SIGNAL NAMES (diagram 7)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destignation (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
HRTC	Horizontal retrace	2	7
VIDEO	Video signal	2	7
VRTC	Vertical retrace	2	7

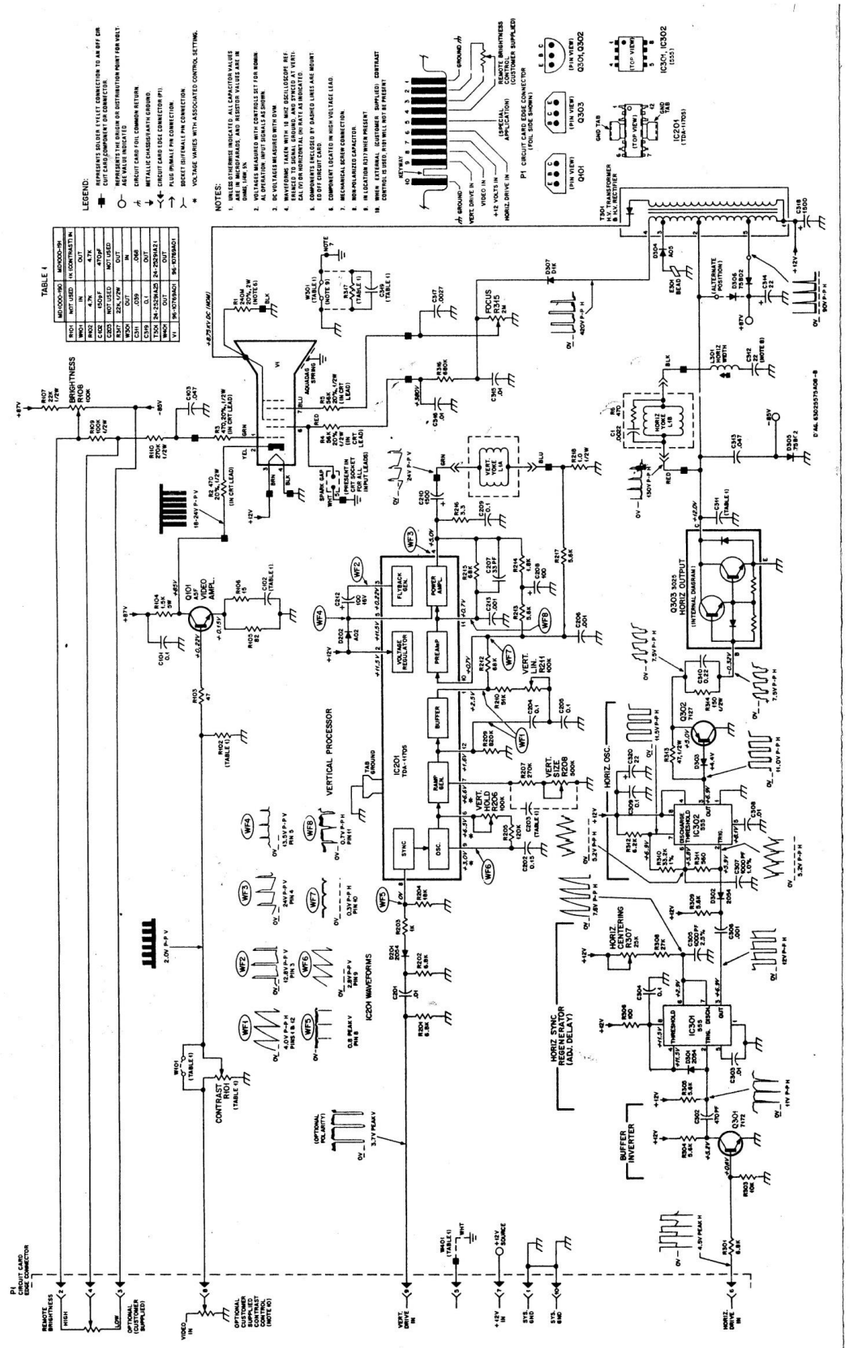
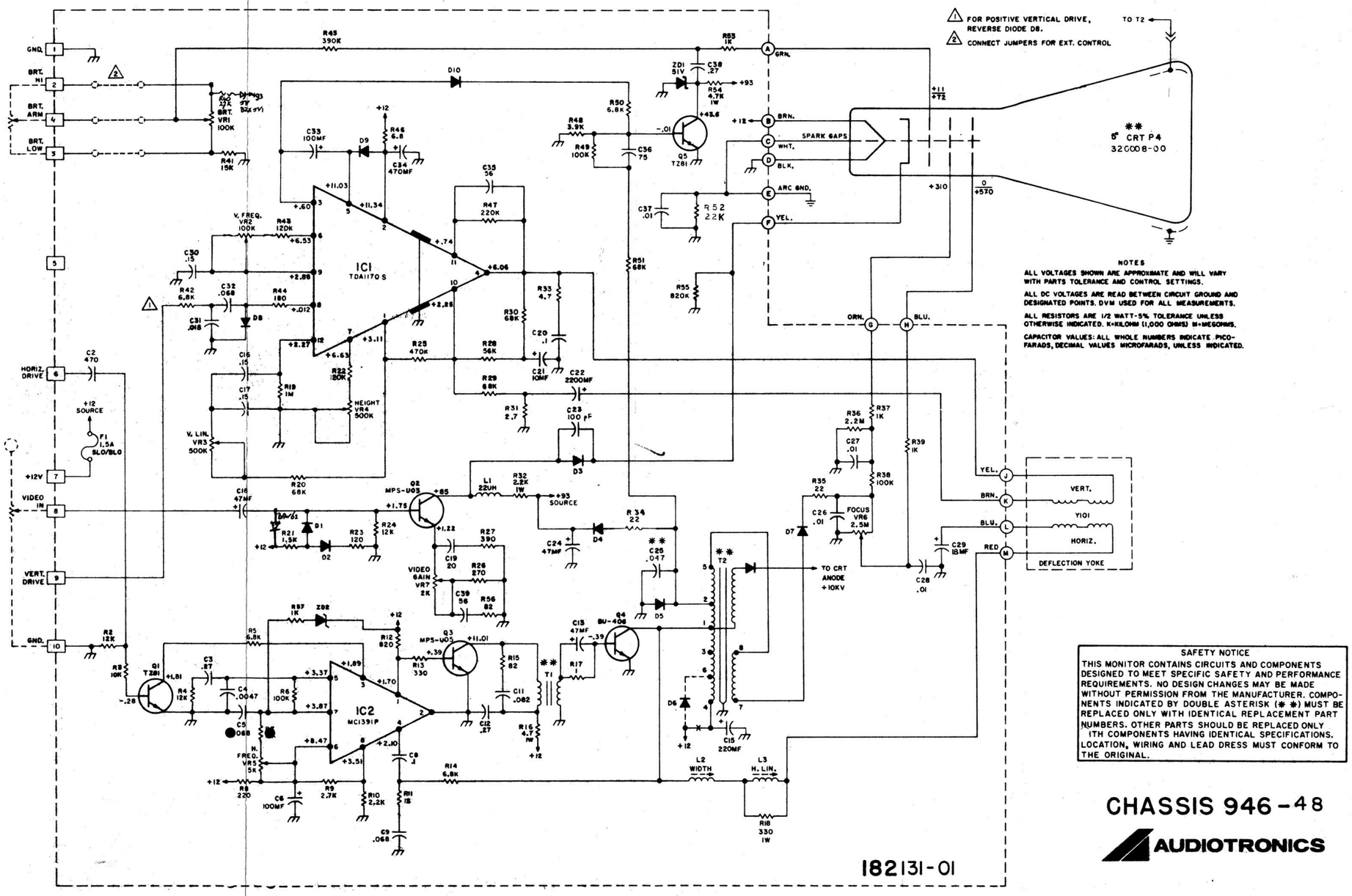


Figure 2.16B : Video display unit 2 (7)



1 FOR POSITIVE VERTICAL DRIVE, REVERSE DIODE D8.

2 CONNECT JUMPERS FOR EXT. CONTROL

NOTES

ALL VOLTAGES SHOWN ARE APPROXIMATE AND WILL VARY WITH PARTS TOLERANCE AND CONTROL SETTINGS.

ALL DC VOLTAGES ARE READ BETWEEN CIRCUIT GROUND AND DESIGNATED POINTS. DVM USED FOR ALL MEASUREMENTS.

ALL RESISTORS ARE 1/2 WATT-5% TOLERANCE UNLESS OTHERWISE INDICATED. K=KILOHM (1,000 OHMS) M=MEGOHMS.

CAPACITOR VALUES: ALL WHOLE NUMBERS INDICATE PICOFARADS, DECIMAL VALUES MICROFARADS, UNLESS INDICATED.

SAFETY NOTICE

THIS MONITOR CONTAINS CIRCUITS AND COMPONENTS DESIGNED TO MEET SPECIFIC SAFETY AND PERFORMANCE REQUIREMENTS. NO DESIGN CHANGES MAY BE MADE WITHOUT PERMISSION FROM THE MANUFACTURER. COMPONENTS INDICATED BY DOUBLE ASTERISK (**) MUST BE REPLACED ONLY WITH IDENTICAL REPLACEMENT PART NUMBERS. OTHER PARTS SHOULD BE REPLACED ONLY ITH COMPONENTS HAVING IDENTICAL SPECIFICATIONS. LOCATION, WIRING AND LEAD DRESS MUST CONFORM TO THE ORIGINAL.

CHASSIS 946-48

AUDIOTRONICS

Figure 2.16C : Video display unit 3 (7)

2.4 POWER SUPPLY

How the power supply is configured in the PM 3632 is shown in figure 2.17.
The power supply is suitable for 50 or 60 Hz and for a wide range of supply voltages.
For setting the supply voltage to 220V or 240V, the transformer is fitted with a pair of fastons (for more details, refer to chapter 7).

The power supply is protected in the following ways:

1. overcurrent
2. overvoltage
3. short-circuit
4. overtemperature: results in overcurrent

The mains voltage passes an EMI filter before it passes the switch and the fuse (in 100V...127V range: 2A delayed. in 200V..250V range: 1A delayed).
The output voltage of the transformer passes a rectifier bridge and is then smoothened to form an unregulated voltage of about 21...23 V.
The zener diode in this line is an overvoltage protection, and a "transient killer" for the power supply circuits.

The secondary side of the transformer is then passed to the switched mode power supply.
The output voltage of the power board is regulated by a varying duty cycle which is under control of the power supply control board.
How the power supply is connected to the other boards in the PM 3632 is shown in figure 2.3.

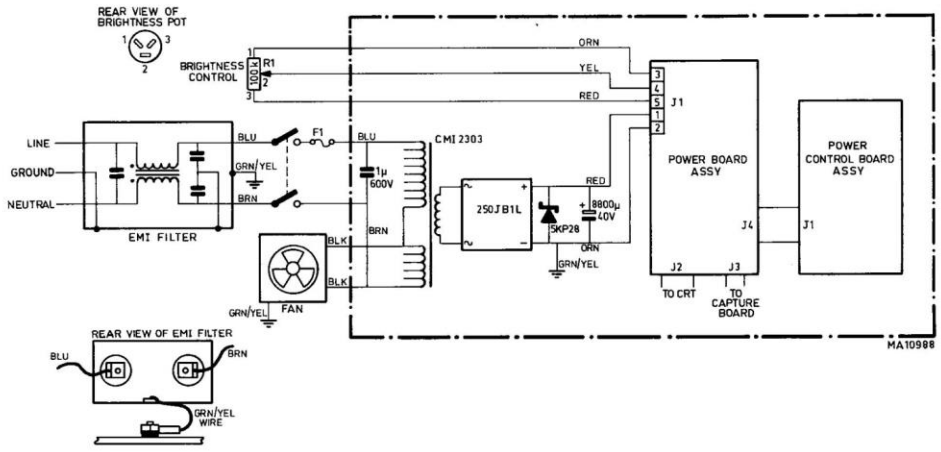


Figure 2.17 : Power supply configuration.

Power board (figure 2.18)

The unregulated voltage comes in at pins 1 (C1+) and 2 (C1-) of connector J1.
This signal passes a 10A fuse and is then distributed to 3 different circuits:

+ 5 V circuit
- 8.5 V circuit
+12 V circuit.

The +5V and -8.5V are switched-mode regulated. The control circuit for these boards is located at the power supply control board.
The output signals of this control board drive power transistors Q3 and Q1.
The +5V circuit consists of:

L3, R8, CR4 : slow-down the collector current increase during switch on.
l4, C5 : 15 kHz filter to smoothen the output voltage.
CR7 : limits the output voltage to +6V in case of no load.
CR6, R9, C4 : limits the collector voltage swing during turn-off.

The -8.5V circuit consist of:

L1, R3, CR1 : slow-down the collector current increase during switch-on.
L2, C3 : 15 kHz filter to smoothen the output voltage.
CR2, R4, C2 : limits the collector voltage swing during turn-off.

The feedback to the power supply control board is done by means of signals +5CL and -8.5Cl.
The +12V supply is not regulated by means of the power supply control board.
This voltage is directly regulated by a 12V regulator and a coil to supress 15 kHz noise.
To increase the capacity of the +12V regulator, transistor Q5 is added.

Power supply control board (figure 2.19)

The control board consists of three sections:

+ 5 V control (U2)
- 8.5 V control (U3)
-12 V generation (U4)

The +5V and -8.5V control circuits are very similar so only the +5V circuit will be described here.

+5V control.

The control circuit for the +5V supply voltage is an SG3524: a regulating pulse width modulator.
The output of this circuit (pin B: +5V DRV) is a signal which is synchronized with the horizontal retrace signal (HRTC) of the video display unit via a one shot (Q1, Q2).
The pulse width of this signal varies according to a varying +5V output voltage. A lower output voltage increases the duty cycle.
A higher output voltage decreases the duty cycle.
This is accomplished via the feedback signal which is applied to operational amplifier U1 (pin2) where it is compared with a reference voltage (formed by the SG3524 itself: pin 16 = +5V).
Diode CR6 affects the duty cycle via pin 10 of the SG3524, but only for transients appearing at the +5V output.
An overcurrent protection is formed by means of operational amplifier U1 (pin8). When the output current becomes too big U1 will affect the duty cycle via pin 4 of the SG3524.
To compensate for noise appearing on the ground, signal SNSRTN (sense return) affects the reference voltage for comparator U1, via R1, C1.

To reduce 50 or 60 Hz noise (coming out of the transformer) the circuit consisting of U1 (pin 7) and associated components also affect the duty cycle, via the feedback input of the SG 3524 (pin 9, signal Vfb-1). Signal ENVFDBK comes from the power board.

Diode CR8, capacitor C21 and associated components take care of a slow start by increasing the duty cycle slowly when powering-up the PM 3632.

-12V generation

The -12V is directly derived from the -8.5V supply.
The principle is that two capacitors (C18 and C19) are switched in parallel by means of Q3 and Q4 and then loaded to -8.5 V (VDD).
Then the capacitors are switched in series which results in a -17 V input voltage for the voltage regulator(VR1).
This voltage regulator provides a -12V output voltage which is then smoothened by means of coil L1.

The switching frequency is synchronized with the switching frequency of the other two control circuits.

NOTE: 1. In earlier instruments, the reset for the 8085 microprocessor is not long enough. This, sometimes, causes the instrument to beep constantly after power-up. To avoid this problem, a modification of the power will cause the power supply to start more quickly.

Change C1 from 10 uF into 0.1 uF:
This causes the +5 V to come-up more quickly.

Change C21 from 10 uF into 100 uF:
Changing C1, causes a too quick start of the +5 V on pin 9 of U2. Changing C21 slows down the Vstart voltage increase.

Replace C15 by a resistor (!) of 4.7 Kohm, 1/4 W, 5 %:
For a more reliable start-up of the -12V supply.

Change R36 from 10 Kohm into 3.3 Kohm:
This causes the a 3.8 V voltage at pin 9 of U4, which sets the switching signal to 50% duty cycle.

2. When having problems with the -12 V supply, replace capacitor C15 by a resistor (!) of 4.7 Kohm, 1/4 W, 5 %. This will result in a more reliable start-up of the -12 V supply.

LIST OF SIGNAL NAMES (diagram 8)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
+5CL	+5 V feedback	8	9
+5VDRV	+5 V drive signal	9	8
-8.5CL	-8.5 V feedback	8	9
-8.5VDRV	-8.5 V drive signal	9	8
ENVFDBK	Feedback for 50 Hz suppression	8	9
HRTC	Horizontal retrace	2	8
SNSRTN	Sense return	8	9
VIDEO	Video signal	2	8
VRTC	Vertical retrace	2	8

LIST OF SIGNAL NAMES (diagram 9)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
+5CL	+5 V feedback	8	9
+5VDRV	+5 V drive signal	9	8
-8.5CL	-8.5 V feedback	8	9
-8.5VDRV	-8.5 V drive signal	9	8
ENVFDBK	Feedback for 50 Hz suppression	8	9
HRTC	Horizontal retrace	2	9
SNSRTN	Sense return	8	9
VFB-1	Feedback voltage	9	9
VSTART	Slow start voltage	9	9

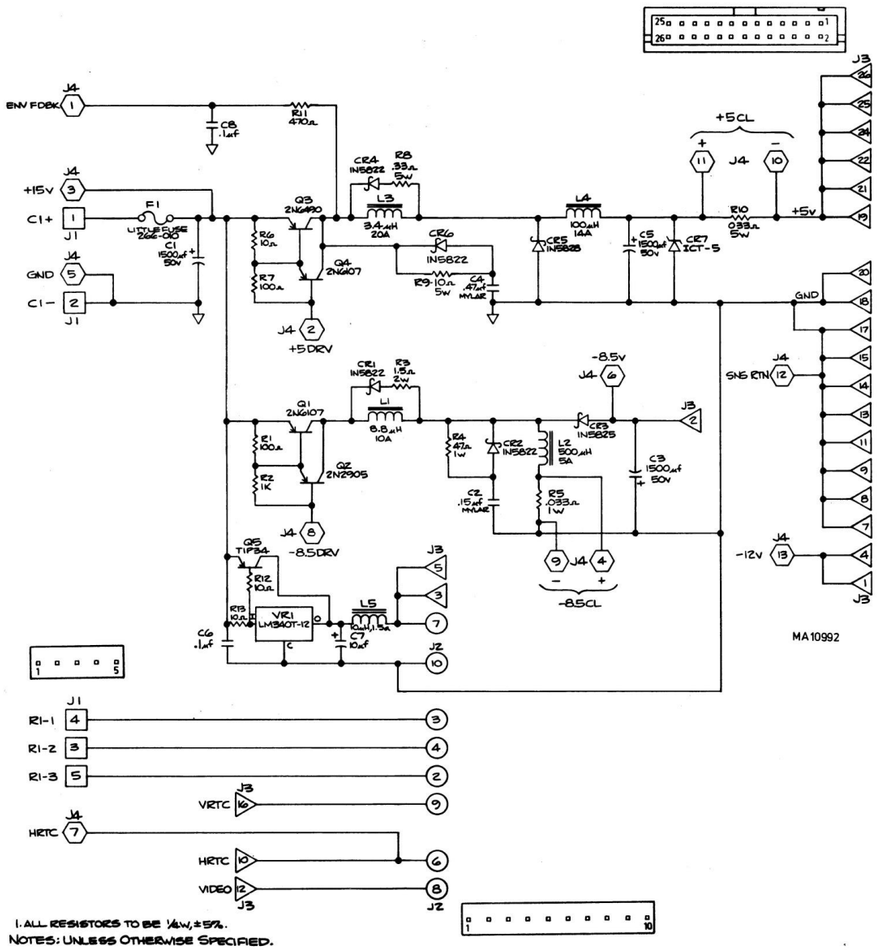
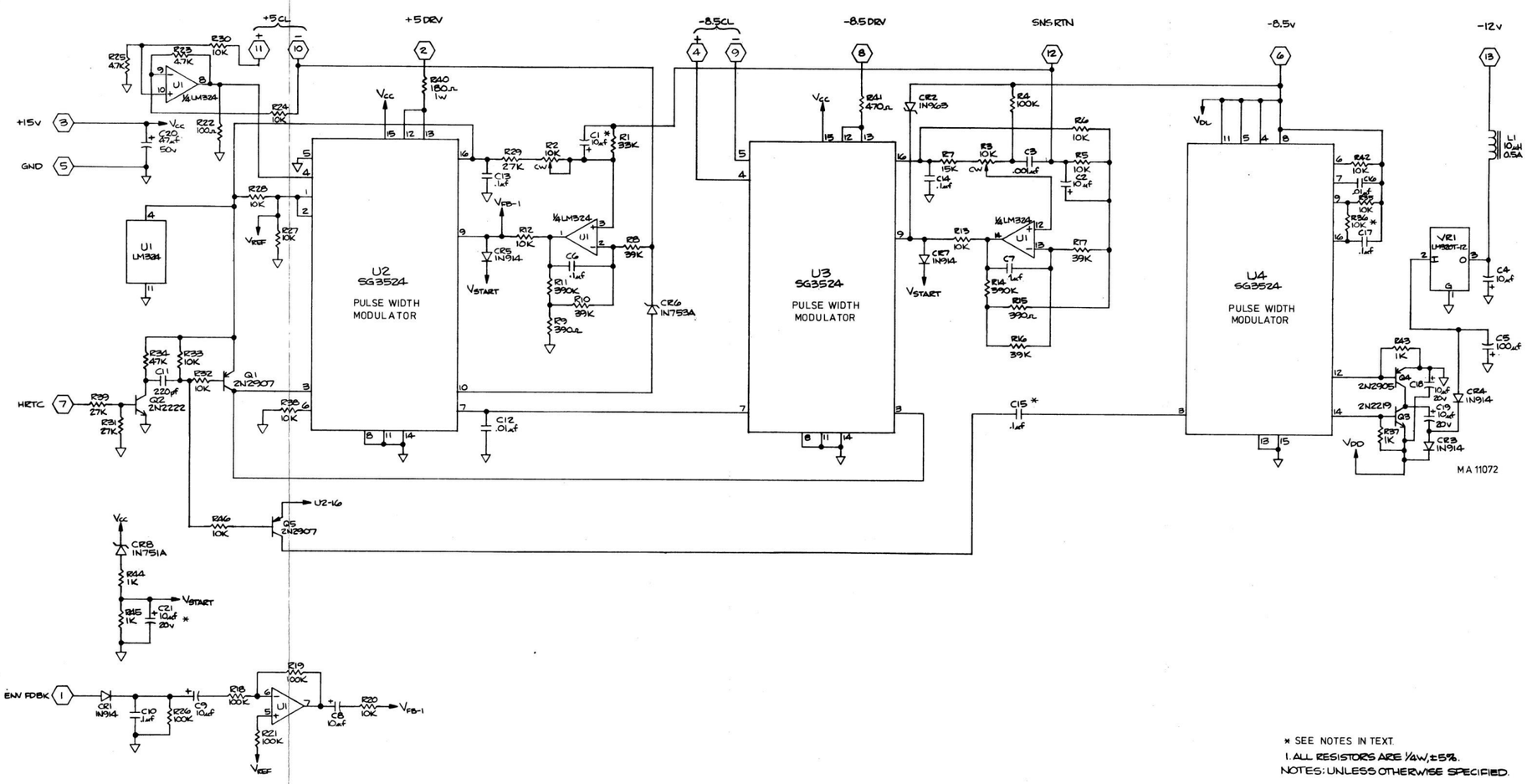


Figure 2.18 : Power supply, power board (8)



* SEE NOTES IN TEXT.
1. ALL RESISTORS ARE ⅛W, ±5%.
NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 2.19 : Power supply, control board (9)

2.5 PARTS LIST PM 3632, MAINFRAME

This list contains all components of the PM 3632 which are not standard.

Some p.c. boards or units are also available from Concern Service, however none of them is listed as a repairable!

NOTE: When ordering the capture board from Concern Service, you will receive the pc board without software. For ordering PROMs, contact the OTE Supply Centre Service Group.
NEDERLANDSE PHILIPS BEDRIJVEN B.V.
MIG S&I, T&M SERVICE DEPARTMENT OTE
BUILDING TQ V-2
EINDHOVEN

POSITION NUMBER	DESCRIPTION	ORDERING CODE
CAPTURE BOARD:		
Capture board, pc board		5322 219 80608
Integrated circuits:		
U37,45,59,60	74F194 SELECTED	5322 209 82418
U57	DELAY 50NS	5322 209 82417
U117	74LS00	5322 209 84823
U101	74LS04	4822 209 80783
U102	74LS08	5322 209 84995
U108	74LS10	5322 209 84996
U104,115	74LS32	5322 209 85311
U114	74LS74	4822 209 80782
U107	74LS86	5322 209 84997
U106	74LS109	5322 209 86522
U103	74LS138	5322 209 85647
U127,132	74LS156	4822 209 80446
U49	74F10	5322 209 81681
U105	74LS163	5322 209 85863
U110	74LS166	5322 209 86292
U119	74LS174	4822 209 81821
U50	74LS245	5322 209 86225
U112	74LS373	5322 209 86062
U24,48,62,63	74F00	5322 209 81534
U56,61,137	74F02	5322 209 81535
U47,128	74F04	5322 209 81577
U32	74F08	5322 209 81574
U129,30	74F20	5322 209 81537
U31,109	74F32	4822 209 82133
U116,123	74F64	5322 209 81538
U58	74F74	5322 209 81474
U39,40,125	74F109	5322 209 81669
U118	74F151	5322 209 81678
U53	74F153	5322 209 81575

POSITION NUMBER	DESCRIPTION	ORDERING CODE
U51,52,126	74F161	5322 209 82001
U41,42,54	74F163	5322 209 82851
U131	74F175	5322 209 81542
U36,64	74F244	5322 209 81128
U10,11,18,19	74F258	5322 209 81769
U26,27,34,35	74F258	5322 209 81769
U44,122	74F374	5322 209 81909
U13,14,21,22	74F399	5322 209 82852
U29,30,38,46	74F399	5322 209 82852
U1-9,17,25	IC 2149	5322 209 10528
U33,124	IC 2149	5322 209 10528
U120	IC 8085A	5322 209 86035
U15,16,134	IC 8155	5322 209 14563
U135,136	IC 8155	5322 209 14563
U133	IC 8276	5322 209 82849
U12,20,28,43	IC 29826	5322 209 82847
U65	74F158	5322 209 81532
U55	CRYSTAL 50 MHZ	5322 242 71206
U23	CRYSTAL 6.2016 MHZ	5322 242 71205
Semiconductors:		
CR01	1N914B	5322 130 31487
Q101	2N2222	5322 130 40221
Q12	2N2369	5322 130 44047
Various:		
C1	CAPACITOR 27PF	4822 122 30045
C4	VAR. CAP. 0-40 PF 250V	5322 125 50278
C5	CAPACITOR 6.8PF	4822 122 31049
L1	100NH CHOKE	5322 158 10682
RP6,101,102	RES. NETWORK 6K8	5322 111 90834
RP1 ... RP5	RES. NETW. 220E/330E	5322 111 90835
J101	CONNECTOR 16 PIN	5322 265 40453
J2	CONNECTOR 26 PIN	5322 265 51106
J3 ... J5	CONNECTOR 36 PIN	5322 265 61055
J6,7	CONNECTOR 25 PIN	5322 290 80648
J1	CONNECTOR 60 PIN	5322 265 61056
KEYBOARD:		
Keyboard, pc board		Not available from C.S.
S1...S39	SWITCHES (CHROME)	5322 273 20207
U1	7407	5322 209 84761
H1	HORN	5322 240 30283
J1	CONNECTOR 16 PIN	5322 265 40453

POSITION NUMBER	DESCRIPTION	ORDERING CODE
POWER SUPPLY, POWER BOARD:		
Power board, pc board		5322 219 80609
Integrated circuits:		
VR1	LM340T-12	4822 209 81019
Semiconductors:		
CR3	1N5825	5322 130 32678
CR5	1N5828	5322 130 32679
Q2	2N2905	5322 130 40021
Q1,4	2N6107	4822 130 40903
Q3	2N6490	5322 130 42507
Q5	TIP 34	5322 130 44334
CR7	TRANSORB.5V 1.5 KW	5322 130 34762
CR1,2,4,6	IN5822	5322 130 32677
Various:		
L5	CHOKE 10UH 1.5A	5322 158 10675
L4	CHOKE 10UH 10A	5322 158 10677
L3	CHOKE 500UH 3.7A	5322 158 10678
L2	CHOKE 3.3UH 20A	5322 158 10679
L1	CHOKE 8.8UH 10A	5322 158 10681
C7	CAPACITOR 10 nF 16V	5322 121 42451
C6, C8	CAPACITOR 0.1 uF 50 V	5322 121 42448
C2	CAPACITOR 0.15 V	5322 121 42449
C4	CAPACITOR 470 nF 100 V	4822 121 41674
C3, C5	CAP. ELCO 1500 uF 25 V	4822 124 40432
C1	CAP. ELCO 1600 uF 40 V	5322 124 41083
R8	RESISTOR 0.33E 5 W	5322 113 60019
J1	CONNECTOR 5 PIN	5322 265 30394
J2	CONNECTOR 10 PIN	5322 265 40452
J4	CONNECTOR 26 PIN	5322 265 51107
F1	LITTLE FUSE 10 A	5322 253 14017
FOR VR1	TO-220 INSULATOR	5322 255 44103
FOR VR1	INSULATING WASHER #4	5322 532 54252
FOR VR1	NYLON NUT	5322 505 10777
FOR VR1	NYLON SCREW	5322 500 10342

POSITION NUMBER	DESCRIPTION	ORDERING CODE

POWER SUPPLY, CONTROL BOARD:

Control board, pc board		5322 219 80611

Integrated circuits:

VR1	LM320T-12	5322 209 82848
U2,3,4	SG3524	5322 209 81508
U1	LM324	4822 209 80587

Semiconductors:

CR8	IN751A	4822 130 34233
CR6	IN753A	4822 130 34167
CR1,3,4,6,7	IN914B	5322 130 31487
Q3	2N2219	5322 130 40496
Q2	2N2222	5322 130 40221
Q4	2N2905	5322 130 40021
Q1,5	2N2907	5322 130 40218

Various:

L1	CHOKE 10UH 0.5A	5322 158 10676
C11	CAPACITOR 220 pF	5322 122 32573
C12, C16	CAPACITOR 0.01 uF 50V	5322 121 42447
C3,6,10,13	CAPACITOR 0.1 uF 50V	5322 121 42448
C14,15,17	CAPACITOR 0.1 uF 50V	5322 121 42448
C1,2,4,8,9,18,19,21	CAPACITOR 10 uF 20V	5322 124 10508
C20	CAPACITOR 47 uF 63V	4822 124 20733
C5	CAPACITOR 100 uF 25V	4822 124 20701
R41	RESISTOR 470E 1/2 W	4822 116 52224
R40	RESISTOR 180E 1.2 W	4822 116 51095
R2, R3	POTENTIOMETER 10K	5322 101 20721

POWER SUPPLY, 'MAINFRAME PARTS'

Transformer 50/60 Hz	5322 148 80195
Zener diode 5KP28	5322 130 32902
Elco 8800 uF 40 VDC	5322 124 41082
Diode bridge	5322 130 32901
Power switch	5322 277 10846
Fan 115 V	5322 361 10321

POSITION NUMBER	DESCRIPTION	ORDERING CODE
CRT MODULE:		
CRT unit (complete)		5322 219 80612
Philips replacements:		
The numbers between brackets are the Philips replacement types.		
Motorola CRT:		
IC201	TDA-1170S (TDA-1170S)	5322 209 86512
IC301, IC302	555 (NE555N)	4822 209 80775
Kaga CRT:		
Q101	2SC2229.0 (2SC22290)	4822 130 41511
Q102, Q401	2SC536 (2SC536C)	4822 130 41063
Q402, Q503	2SD600K (2SD600)	4822 130 41141
Q501, Q502	2SC930 (2SC930NPD)	4822 130 41597
Q504	2SC2373 (2SC2373L)	4822 130 41566
IC401	uPC1031H2 (UPC1031HA)	4822 209 80528
Audiotronix CRT:		
Q2	MPS-U03 (MPS-U03)	5322 130 44327
Q3	MPS-U05 (MPS-U05)	5322 130 44562
Q4	BU-406 (BU-406)	5322 130 44581
IC1	TDA1170S (TDA1170S)	3222 209 86512
MECHANICAL:		
Option card retainer		5322 405 90284
Handle assembly		5322 498 70066
Cabinet bezel, front		5322 447 90448
Cabinet bezel, back		5322 447 90447
CRT bezel		5322 466 60976
Front panel		5322 447 90449
Back panel		5322 447 90451
Fan cover + filter		5322 447 90577
Top cover		5322 447 90578
Bottom cover		5322 447 90579

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